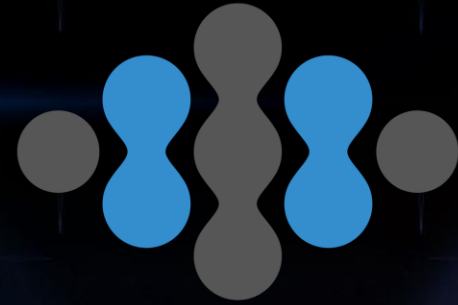




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Investor Presentation

November 2025

This presentation contains forward-looking statements concerning Atomera Incorporated (“Atomera,” the “Company,” “we,” “us,” and “our”). The words “believe,” “may,” “will,” “potentially,” “estimate,” “continue,” “anticipate,” “intend,” “could,” “would,” “project,” “plan,” “expect” and similar expressions that convey uncertainty of future events or outcomes are intended to identify forward-looking statements. These forward-looking statements are subject to a number of risks, uncertainties and assumptions, including those disclosed in the section “Risk Factors” included in our Annual Report on Form 10-K filed with the SEC on March 4, 2025 (the “Annual Report”). In light of these risks, uncertainties and assumptions, the forward-looking events and circumstances discussed in this presentation may not occur and actual results could differ materially and adversely from those anticipated or implied in our forward-looking statements. You should not rely upon forward-looking statements as predictions of future events. Although we believe that the expectations reflected in our forward-looking statements are reasonable, we cannot guarantee that the future results, levels of activity, performance or events and circumstances described in the forward-looking statements will be achieved or occur.

This presentation contains only basic information concerning Atomera. The Company’s filings with the Securities Exchange Commission, including the Annual Report, include more information about factors that could affect the Company’s operating and financial results. We assume no obligation to update information contained in this presentation. Although this presentation may remain available on the Company’s website or elsewhere, its continued availability does not indicate that we are reaffirming or confirming any of the information contained herein.

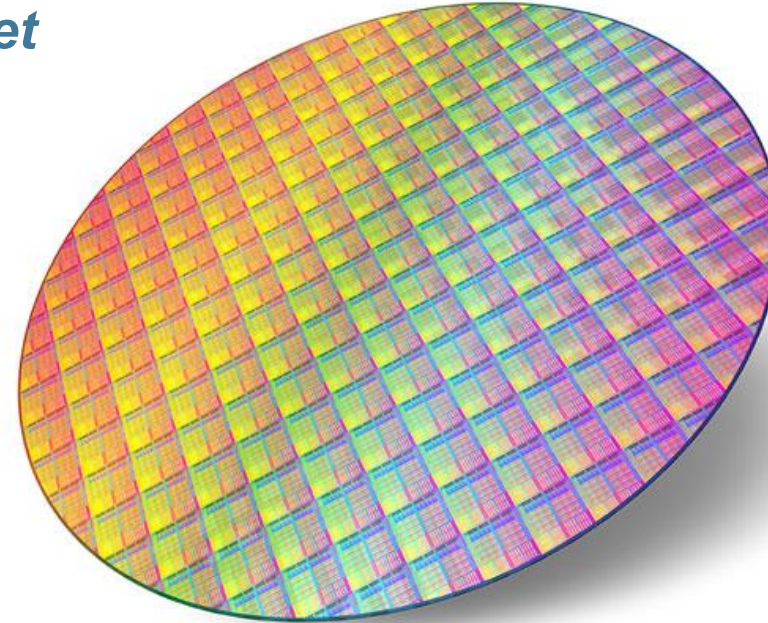
Mears Silicon Technology (MST®)

Quantum Engineered Materials



Transistor enhancement technology for the \$600B semiconductor market

High Leverage IP Licensing Business Model



Top Tier Management Team

Strong, Growing and Defensible Patent Portfolio

Potential Benefits

► Improved Efficiency

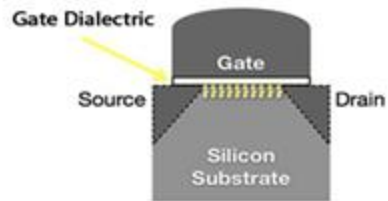
- Higher transistor performance
- Lower power consumption
- Better reliability

► Lower cost

- Reduced die size
- Improved yield
- Higher throughput

► Same benefits as a node shrink

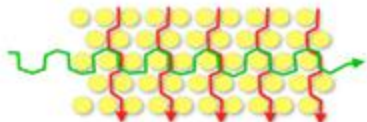
STANDARD SILICON TRANSISTOR



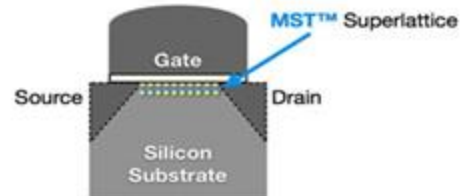
Standard Silicon
Atomic Structure



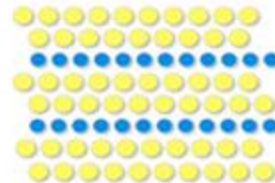
LIMITED Horizontal Current Flow +
EXCESSIVE Vertical Leakage



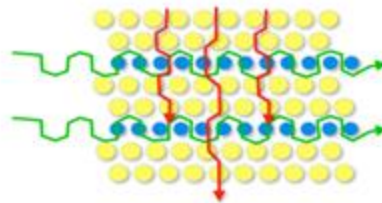
MST SILICON TRANSISTOR



MST™ Silicon
Atomic Structure



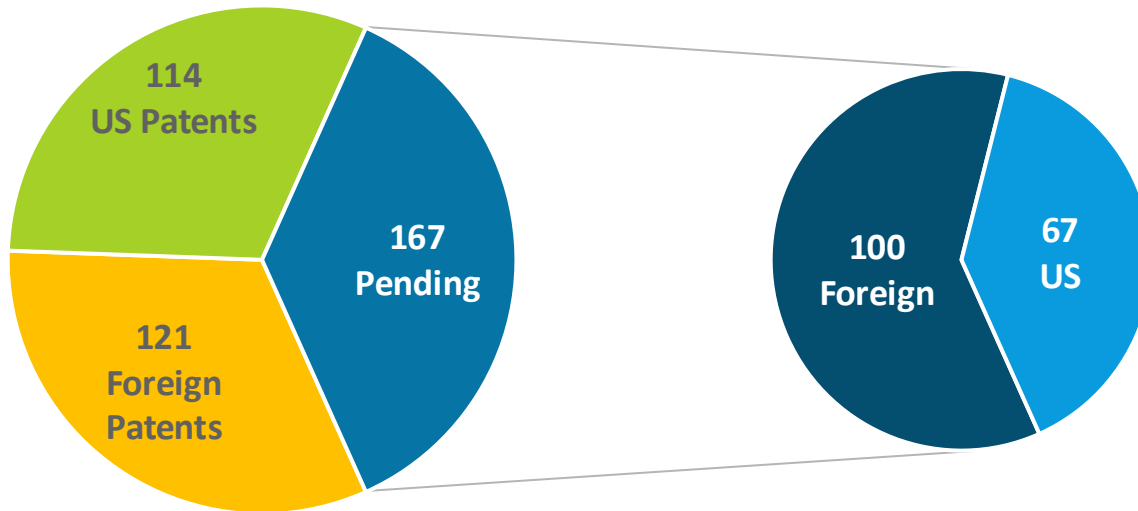
INCREASED Horizontal Current Flow +
REDUCED Vertical Leakage



Strong and Growing IP Portfolio



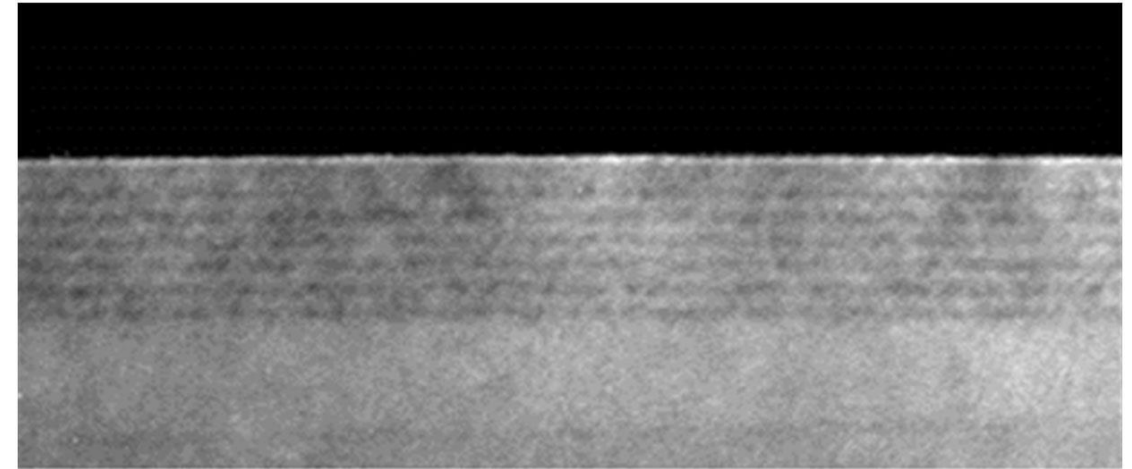
402 Patents Issued and Pending



Core MST Method and Device
MST Enabled Devices/Architecture
Next-Gen Architectures using MST

Discoverable

These distinctive layers are visible on products using MST



Extensive know-how

Extends life and value of patents

Target Customers & Partners



Integrated Device Manufacturers



Foundry



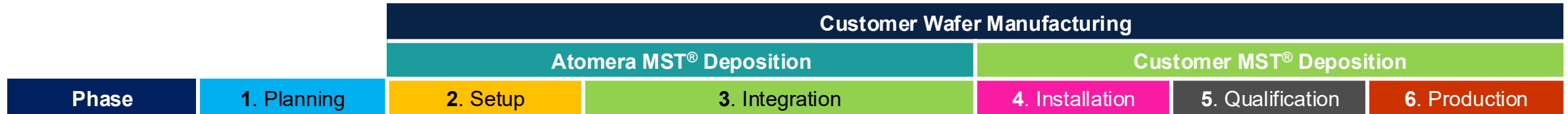
Fabless



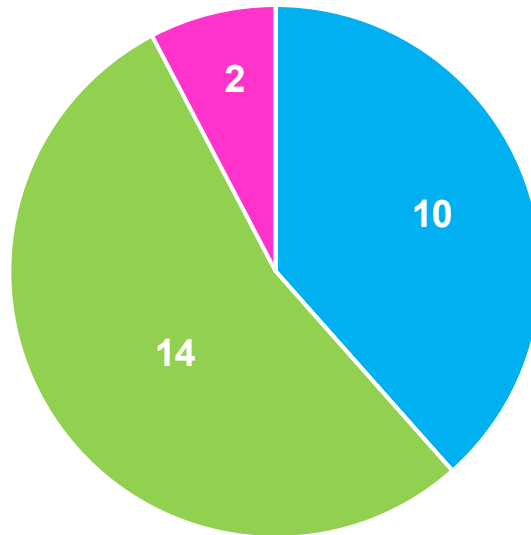
Tool Suppliers (Partners)



Customer Status



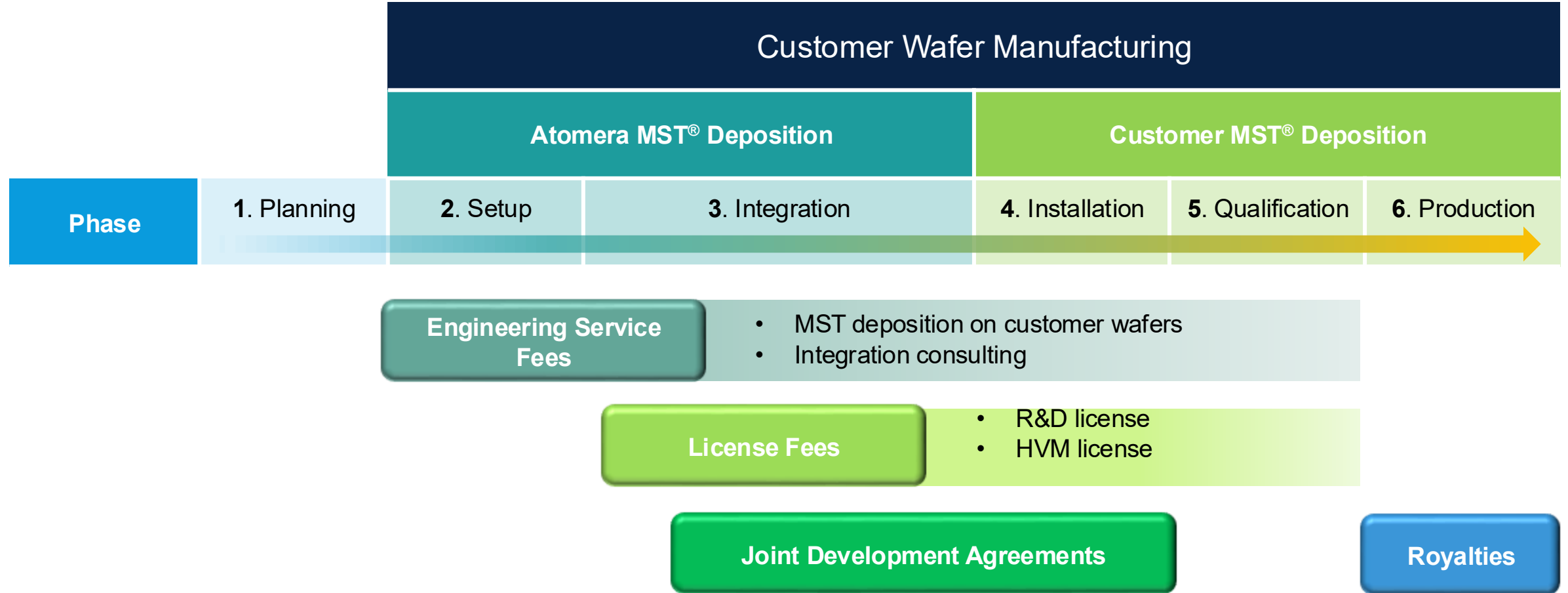
Engagement Phases



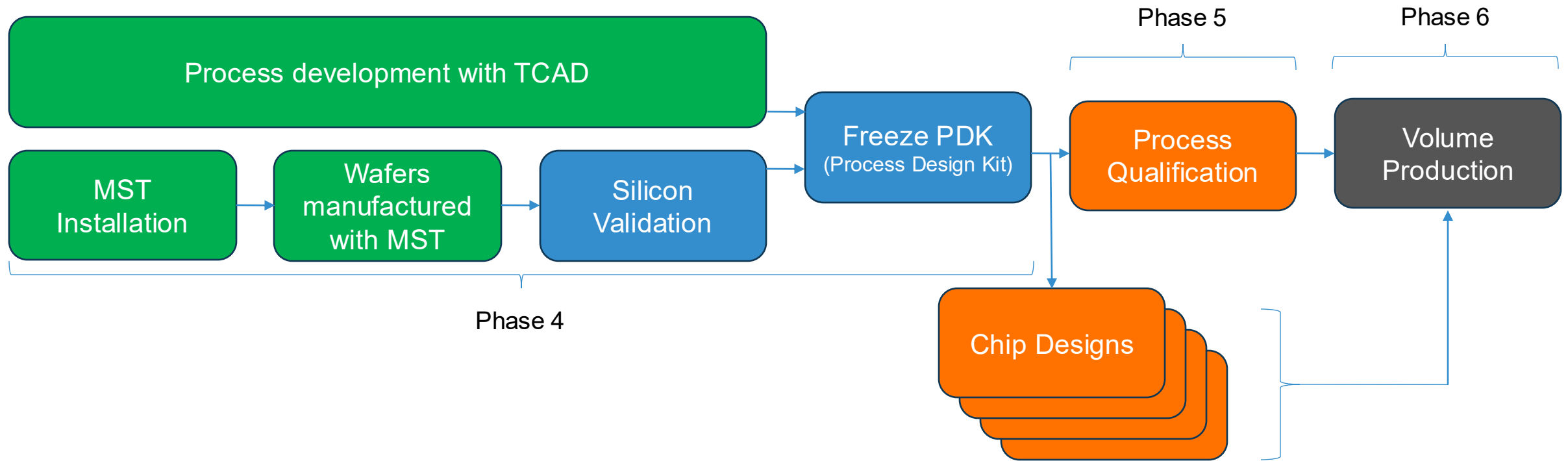
- 20 customers, 26 engagements
- Working with more than half of the world's top semiconductor makers*

• At least 10 of the top 20 semiconductor sales leaders with fabs (IC Insights, McClean Report 2023)

Customer Engagement & Revenue Model



Productization cycle



Revenue potential and timing



MST starting wafers

Easier integration, faster time to revenue

- RFSOI, GaN, Next Gen DRAM, etc



High volume potential products

Longer integration, higher revenue potential

- GAA Logic, DRAM, Power, Flash memory, etc.

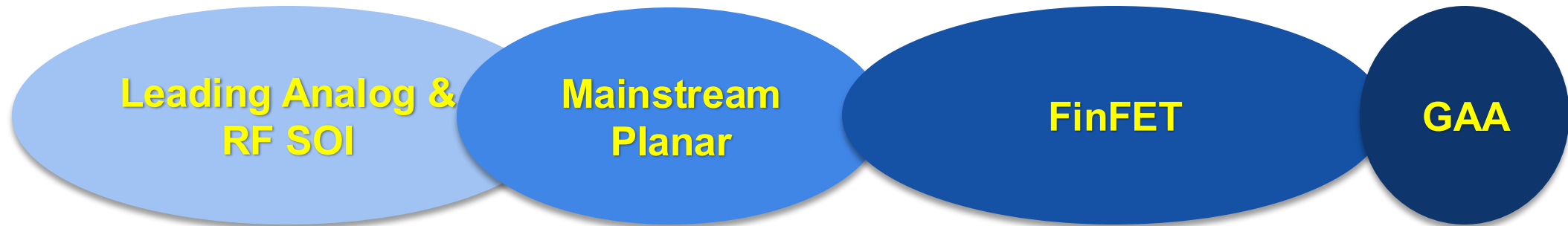


Breakthrough, enabling materials

New disruptive technologies

- Si28 for Quantum, Piezo, HBM Memory, etc.

MST Key Benefits Across Nodes



Mobility	8%	20%	25%	10%	15+%
Dopant Engineering	20%	15%	15%	15%	20%
Reliability (TDDDB/BTI)	25%	25%	25%	25%	25%

← 180nm 130nm 90nm 65nm 40nm 28nm 22nm 16/14nm 10nm 7nm 5nm 2nm →

These Benefits are ADDITIVE & COMPLEMENTARY to other enhancement technologies

MST technology focus areas



MST-SP,
SPX for
BCD

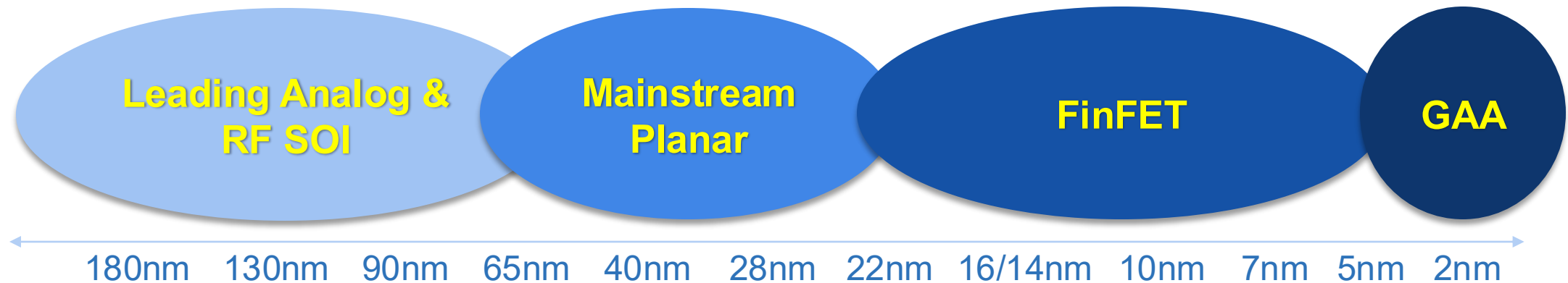
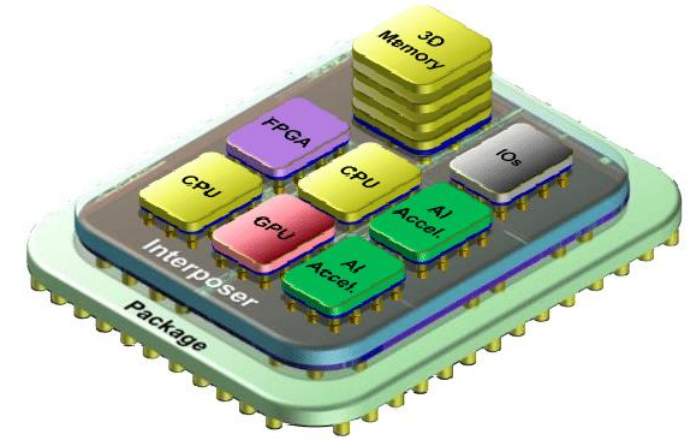
MST for
RF-SOI

MST for
Advanced
Nodes

MST for
DRAM

MST optimizes AI performance

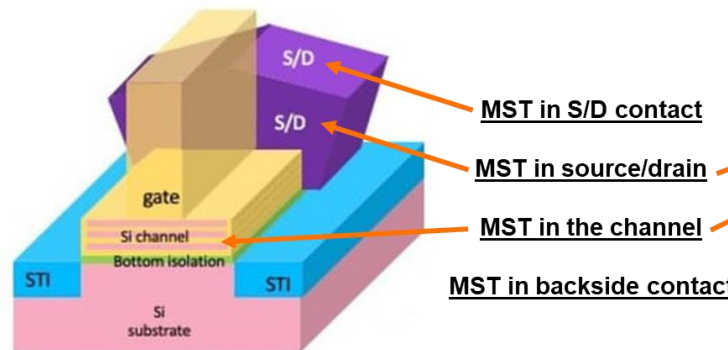
- ▶ **AI algorithms are driving unparalled computing demands**
 - Exceeding ideal single chip silicon area which impacts yield
- ▶ **Heterogenous chiplet architectures solve this problem**
- ▶ **Small chiplet designs can be optimized by process node**
- ▶ **MST's ability to enhance mature nodes brings great value**



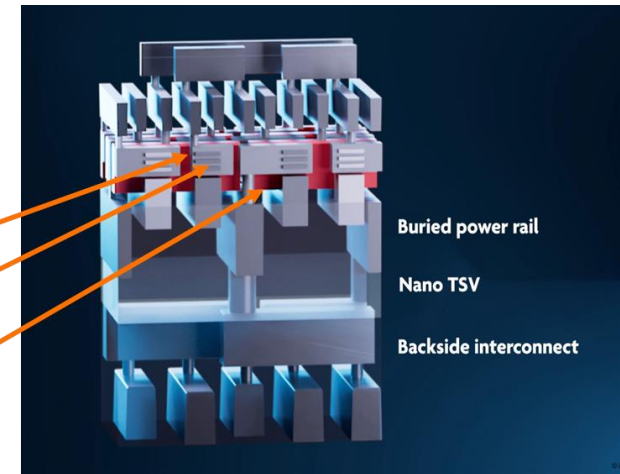
Strategic Marketing Agreement



- ▶ Joint marketing agreement with major semiconductor equipment maker
- ▶ Focused on Gate-All-Around transistors
- ▶ Enables solutions that are more validated so faster to production
- ▶ Leverages partner's sales and marketing resources
- ▶ Partnership may extend into other application areas



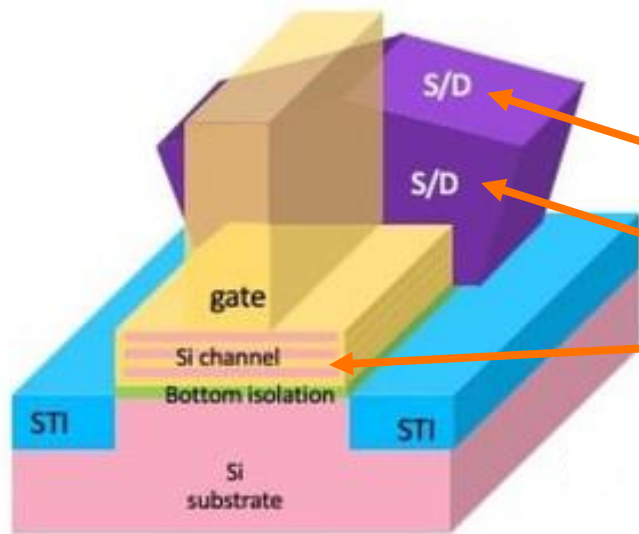
Source: S. Mukesh, Electronics (2022)



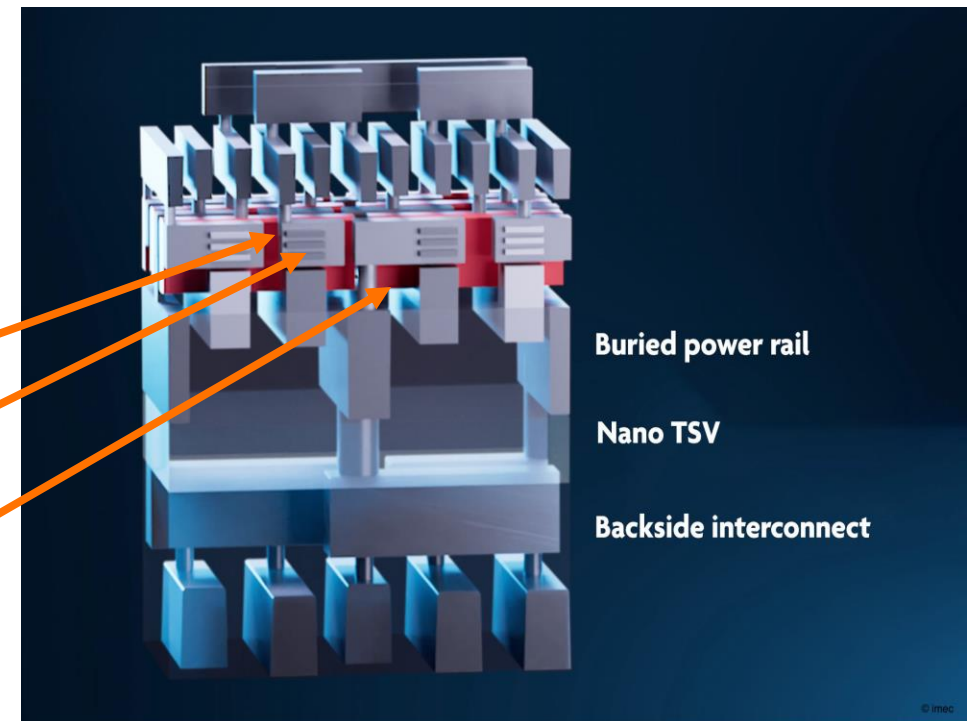
Source: IMEC

GAA Opportunity

- ▶ MST provides benefits in multiple areas for Gate-All-Around transistors

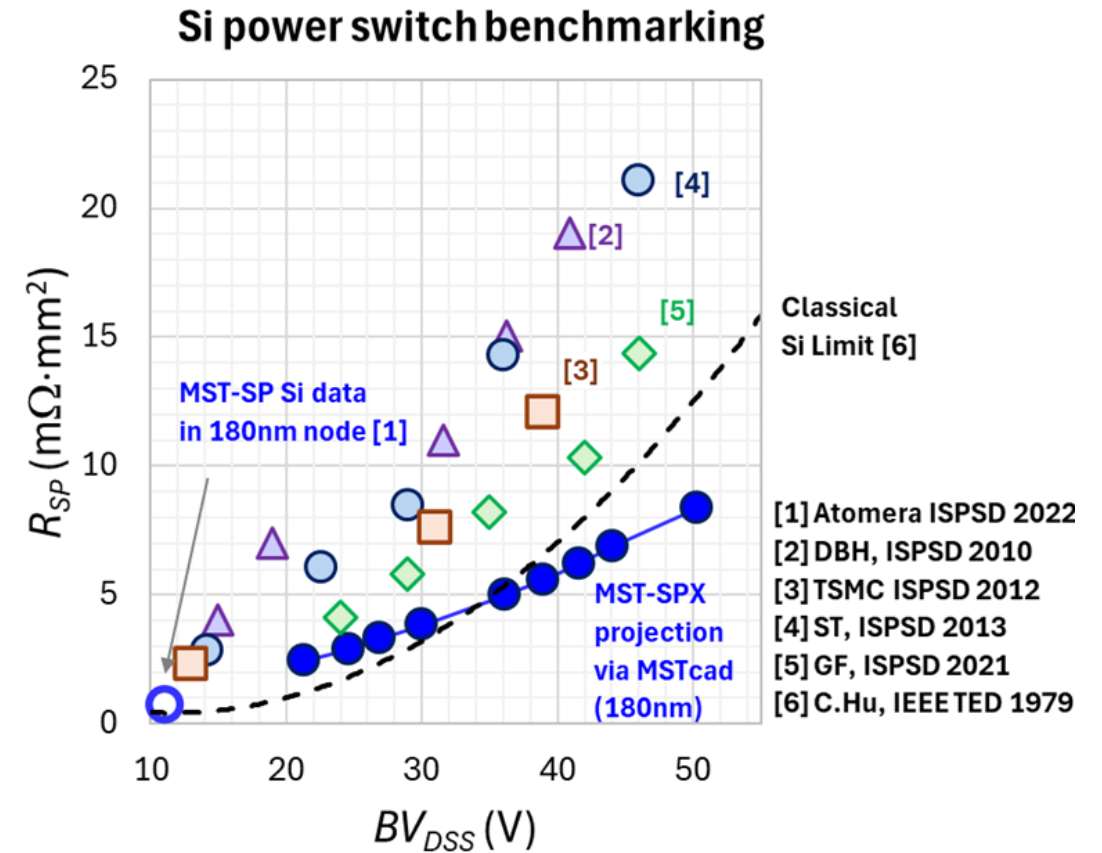


Source: S. Mukesh, Electronics (2022)



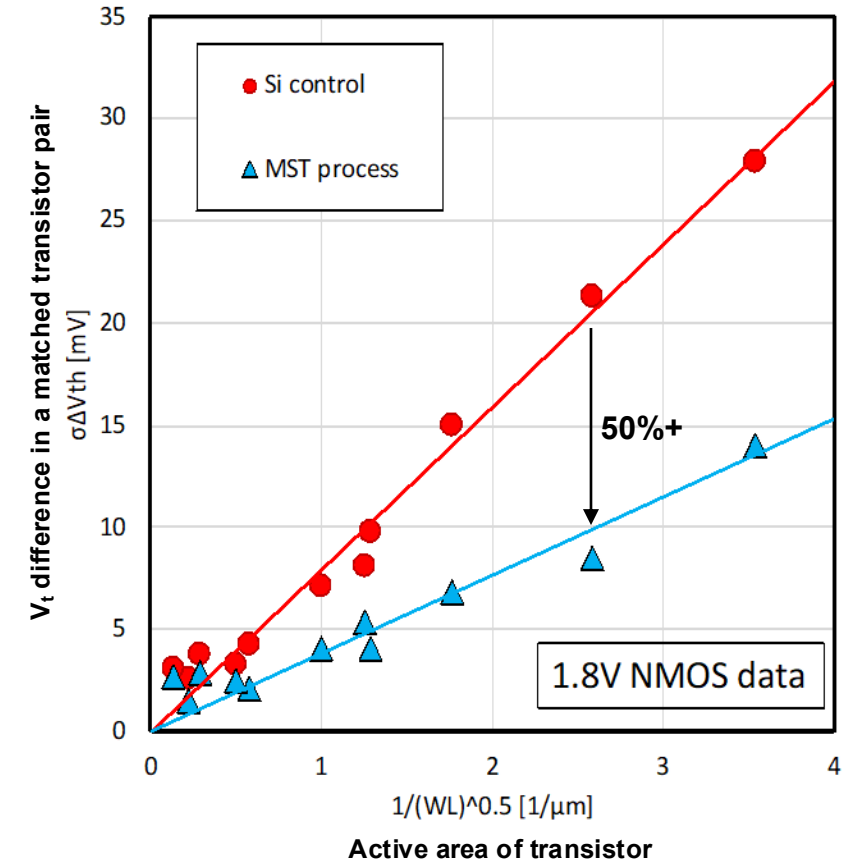
Source: IMEC

- ▶ **Atomera introduced MST-SP in 2022**
 - Market leading 5V R_{sp} vs BV_{dss} performance
 - Allows higher efficiency, smaller size
- ▶ **MST-SPX targets 5-48V**
 - Area of highest customer interest
- ▶ **MST achieves best in class performance**
 - MST-SPX beat all published results
 - Simulations predict up to 20% improvement
 - Customers have simulated higher levels
- ▶ **Provides clear economic benefit to customers**



Variability reduction with MST

- ▶ **High variability between transistors is a significant issue**
 - A big driver of variability is Random Dopant Fluctuation (RDF)
 - Some transistors are designed larger to account for variability
 - This increases costs and limits the minimum achievable voltage and power
- ▶ **Advanced GAA transistor need solutions for RDF**
- ▶ **DRAM sense-amp variability is a major design constraint**
 - Sense-amp margin defines refresh interval and resulting power
 - Improving variability allows smaller sense-amp and reduced power
- ▶ **MST can minimize RDF and lower variability, critical in advanced nodes and memories**





▶ **Macro factors affecting handset design**

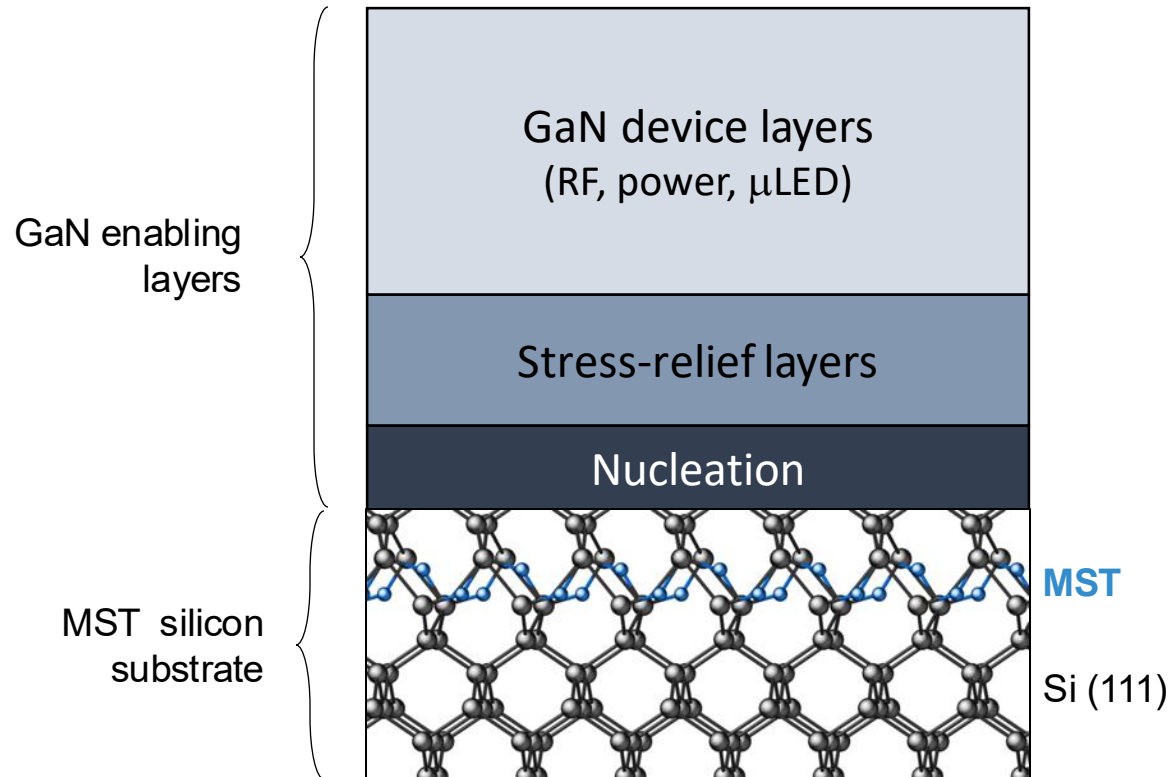
- New mobile phones want to move from 4 to 6 carrier aggregation channels
- New freq bands opening for 5G and 6G cellular

▶ **LNAs (Low Noise Amplifiers)**

- Receiver circuit used in mobile phones
- Must turn on frequently to monitor for signals
- Can be a major source of power consumption
- Even more bands/channels coming soon

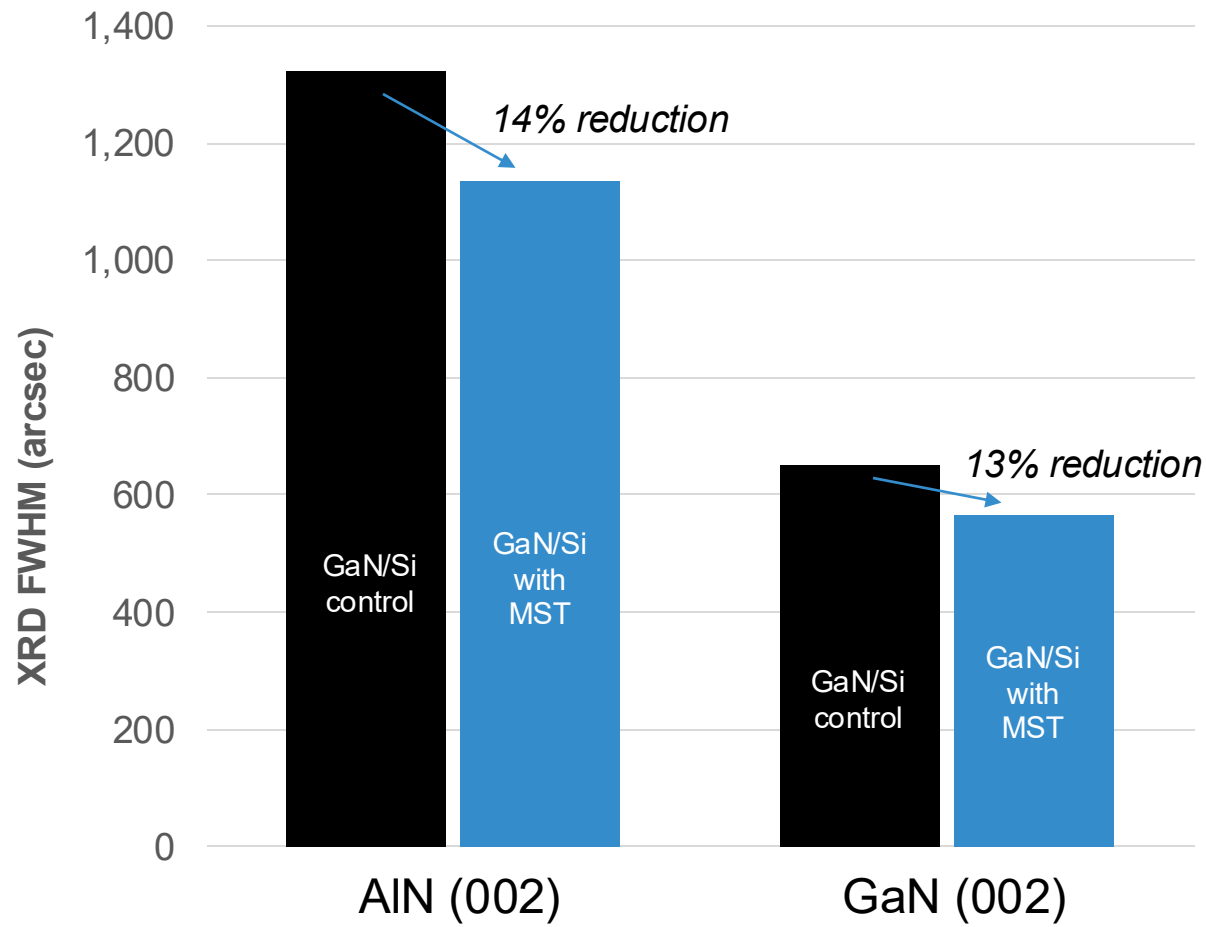
▶ **Leading handset makers seeking much lower power LNAs which MST can help deliver**

MST for GaN/Si



- ▶ Atomera provides modified Si substrates incorporating MST layers
- ▶ GaN growth at various US locations
- ▶ Physical characterization indicates fewer defects in GaN device layer
- ▶ Electrical characterization in process at Sandia National Lab
- ▶ Preliminary electrical data is consistent with lower defects (lower leakage, higher breakdown voltage)
- ▶ Sandia National Lab Rapid Access Program renewed in April 2025

GaN/Si crystal quality improvement



X-ray confirms crystal quality improvement with MST

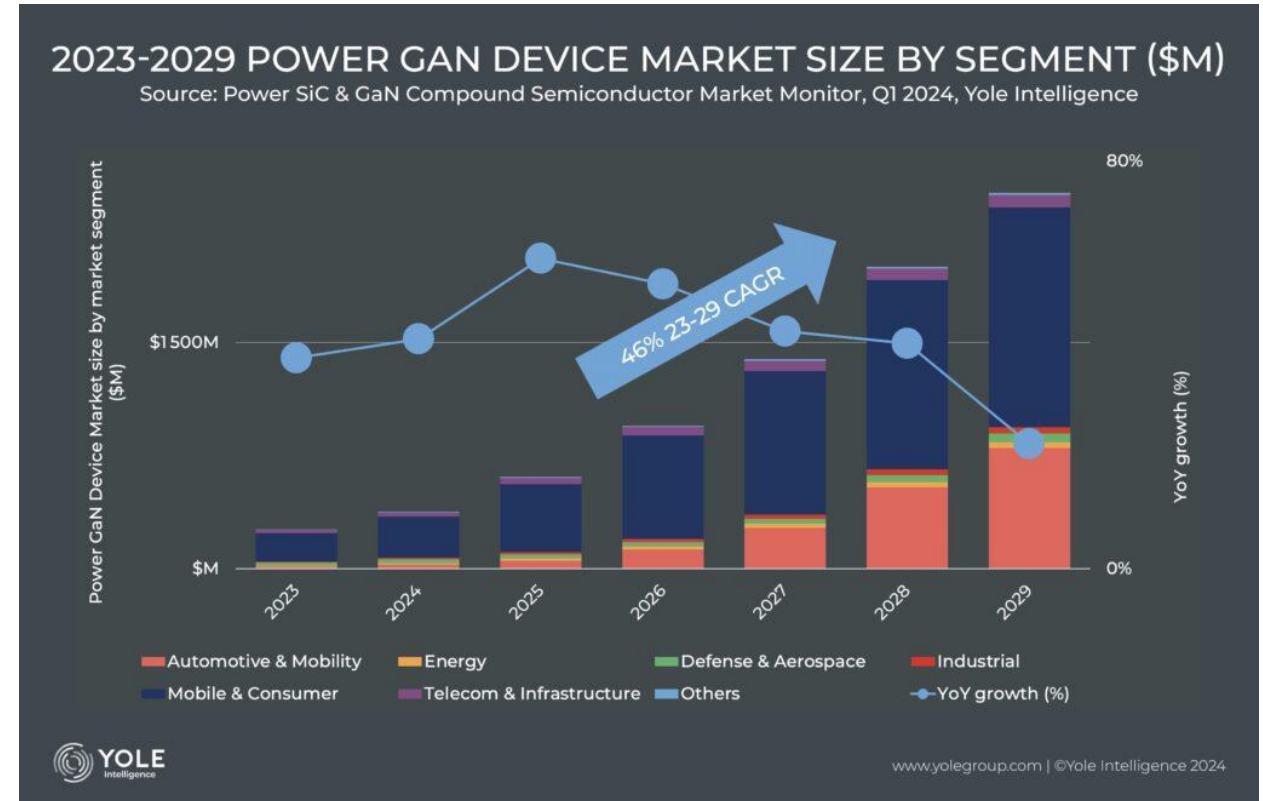
Collaboration with Sandia's CINT to validate benefits



In plot, each bar represents the average of FWHM values measured at positions 15mm and 30mm from the center of a 100mm wafer

Compound Semiconductors

- ▶ **Compound semiconductor market growing rapidly**
 - GaN is one example
- ▶ **Poor wafer substrate quality causes manufacturing challenges**
- ▶ **Atomera's MST may help to solve this problem**
- ▶ **Early experiments of GaN on MST show promising results**



Royalty Opportunity



- ▶ ~410 wafer fabs operating worldwide
- ▶ Adoption of MST in one fab can make Atomera profitable from royalties alone
 - 2025 non-GAAP OPEX guidance is ~\$17M

Example 1 Worldwide Average Fab	
Monthly Fab Capacity ¹ (wafers/month)	46,240
Industry average wafer ASP - 2018	\$1,365
Annual Revenue Potential²	\$15.1M
Annual Revenue at 50% of ramp ²	\$7.6M

Example 2 Leading Foundry, 28nm Fab	
Monthly Fab Capacity (wafers/month)	80,000
Industry average 28nm wafer ASP	\$3,300
Annual Revenue Potential²	\$63M
Annual Revenue at 50% of ramp ²	\$31.7M

1. Represents wafers starts per month (200mm equiv) – 227.5M starts in 410 fabs

2. Assumes 2% royalty rate

Source: IC Insights Global Wafer Capacity 2021-2025 report, McClean Report 2021, 2022

MST Customer Business Opportunity



► Foundry economics

	Wafer Price	GM%	GM\$ Increase	MST Royalty	Wafer Cost	
28nm HP wafer	\$ 3,300	45%	\$ -	\$ -	\$ 1,815	
28nm HP+ wafer	\$ 3,450	45%	\$ 68	\$ -		5% higher price for +15% performance boost
28nm HP wafer with MST	\$ 3,600	47.0%	\$ 208	\$ 72	\$ 1,907	30% performance boost=10% higher price (+ \$20 MST cost)
28nm HP wafer with MST	\$ 3,713	48.6%	\$ 318	\$ 74	\$ 1,909	25% die shrink=12.5% price increase (+ \$20 MST cost)

- **Gross margin increases by \$200-\$300 per wafer after foundry pays Atomera royalties**

► Fabless semiconductor economics

	Chip sales/ wafer	GM%	GM\$ Increase	Product ASP	Die/wafer	
28nm HP wafer	\$ 9,233	50%	\$ -	\$ 4.86	2,235	Baseline business for 30mm ² chip
28nm HP wafer with MST	\$ 12,398	59%	\$ 3,165	\$ 4.86	3,001	Improved financials with 25% size reduction

- **Sales and profit both increase by over \$3000 per wafer for fabless manufacturer**

► Everyone in the value chain benefits from MST technology

Financial Review



Income Statement

(\$ in thousands, except per-share data)

	Three Months Ended		
	September 30, 2025	June 30, 2025	September 30, 2024
REVENUE	\$ 11	\$ -	\$ 22
Gross Profit	(117)	(62)	19
OPERATING EXPENSES			
Research & Development	3,304	3,004	2,759
General and Administration	2,165	2,048	1,812
Selling and Marketing	207	141	248
TOTAL OPERATING EXPENSES	5,676	5,193	4,819
OPERATING LOSS	(5,793)	(5,255)	(4,800)
Other Income (Expense)	220	288	205
NET LOSS	\$ (5,573)	\$ (4,967)	\$ (4,595)
Net Loss Per Share	\$ (0.19)	\$ (0.17)	\$ (0.17)
Weighted average shares outstanding	31,128	30,397	27,406
ADJUSTED EBITDA (NON-GAAP)	\$ (4,440)	\$ (3,965)	\$ (3,881)
ADJUSTED EBITDA PER SHARE	\$ (0.14)	\$ (0.13)	\$ (0.14)

Balance Sheet Information

Cash, equivalents & ST investments	\$ 20,322	\$ 22,026	\$ 17,342
Debt	-	-	-

Summary

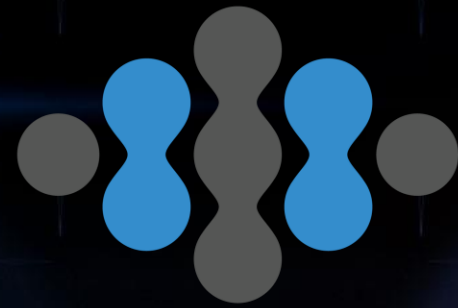


- ▶ High margin, recurring revenue financial model
- ▶ Strong technology, patent position, and balance sheet
- ▶ Traction with many top industry players and growing licensee base
- ▶ Ramping commercial license revenues



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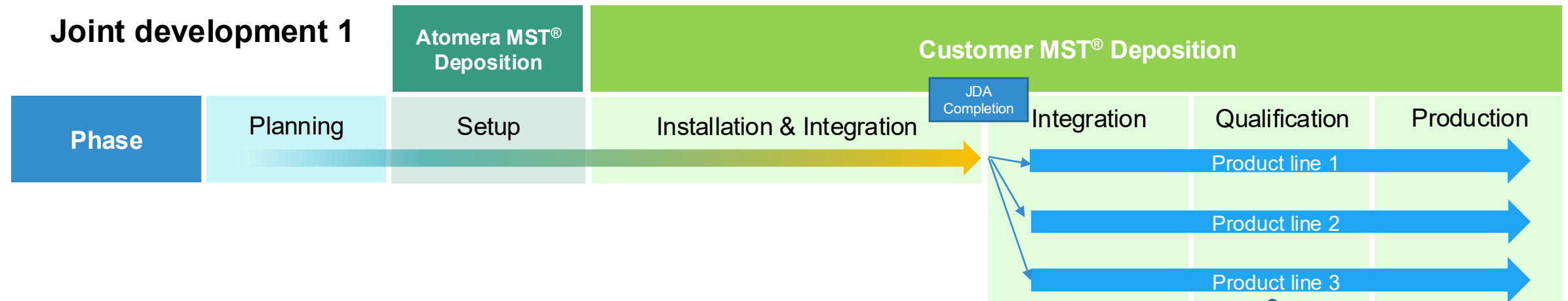
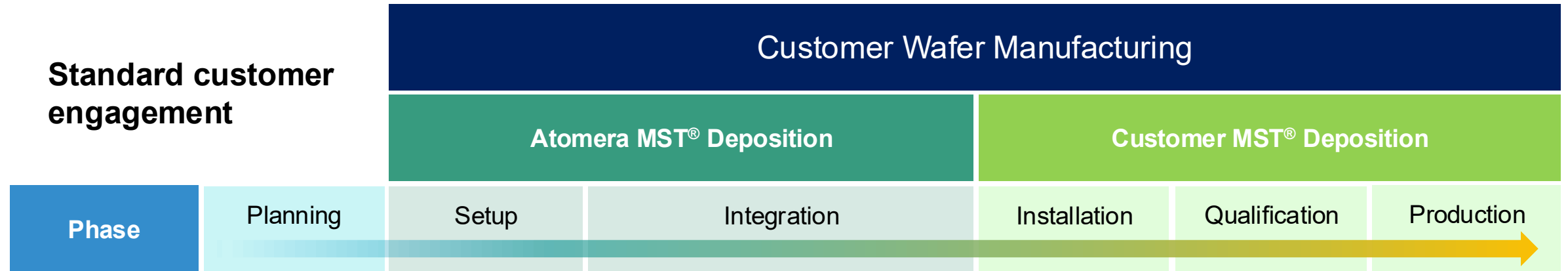
Thank You



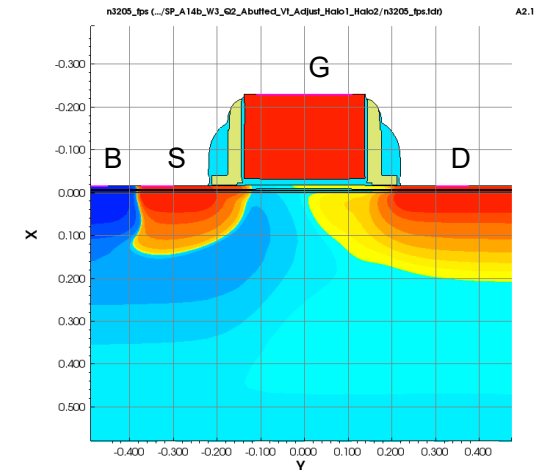
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Backup Slides

Customer Engagement Model



- ▶ **MST-SP is a highly-engineered asymmetric power device**
 - Uses MST to enhance I_{dlin} and precisely control dopant profiles
- ▶ **Improves 5V power devices**
 - Lower R_{SP}
 - Can be traded for up to 20% smaller area
- ▶ **Targeted for rapidly-growing PMIC market**



5V Transistors – Critical and Growing Market

- ▶ **Targeted at rapidly-growing PMIC (Power Management IC) market**
 - Power devices can be up to 80% of PMIC die area
- ▶ **All ICs need stable, regulated power**
 - Across battery charge level, lifetime degradation, and load
 - Across usage modes – DVS (Dynamic Voltage Scaling), sleep, others
- ▶ **5V transistor required to deliver IC power from any source**
 - Battery-powered, USB, wall connected
- ▶ **5V devices do not scale with Moore's Law**
- ▶ **MST SP allows significant scaling of gate length, and a performance boost**

2018-2025F IC Market Forecast by Device Type (Analog)

Product Category	18	19	19/18 % Chng	20	20/19 % Chng	21F	21/20 % Chng	22F	22/21 % Chng	23F	23/22 % Chng	24F	24/23 % Chng	25F	25/24 % Chng	20-25 CAGR
Power Management (\$M)	14,529	14,050	-3%	14,640	4%	18,153	24%	20,332	12%	22,568	11%	23,019	2%	24,861	8%	11%
Units (M)	69,243	67,227	-3%	68,409	2%	80,788	18%	91,396	13%	102,475	12%	105,580	3%	115,178	9%	11%
ASP (\$)	\$0.21	\$0.21	0%	\$0.21	2%	\$0.22	5%	\$0.22	-1%	\$0.22	-1%	\$0.22	-1%	\$0.22	-1%	0%

Source: IC Insight's McClean Report, June 2021

THE WALL STREET JOURNAL.

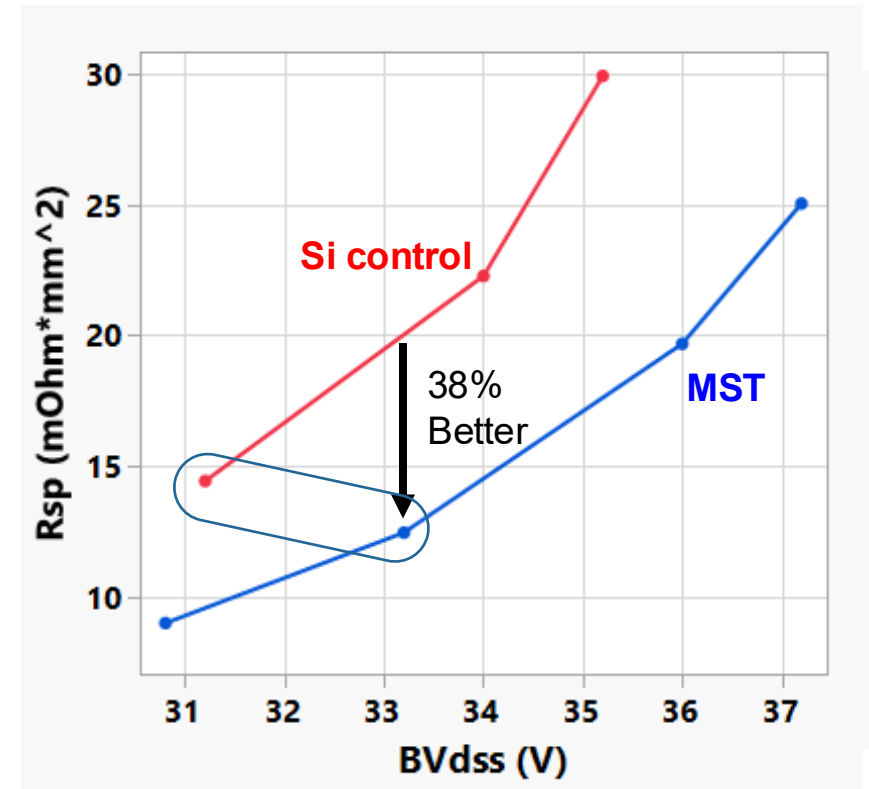
"A typical 5G smartphone can hold as many as eight power-management chips, compared with two to three in a 4G phone, according to Hui He, an analyst at research firm Omdia."

WSJ "Why the Chip Shortage is So Hard to Overcome" 4/20/2021

MST-SPX targeting power devices

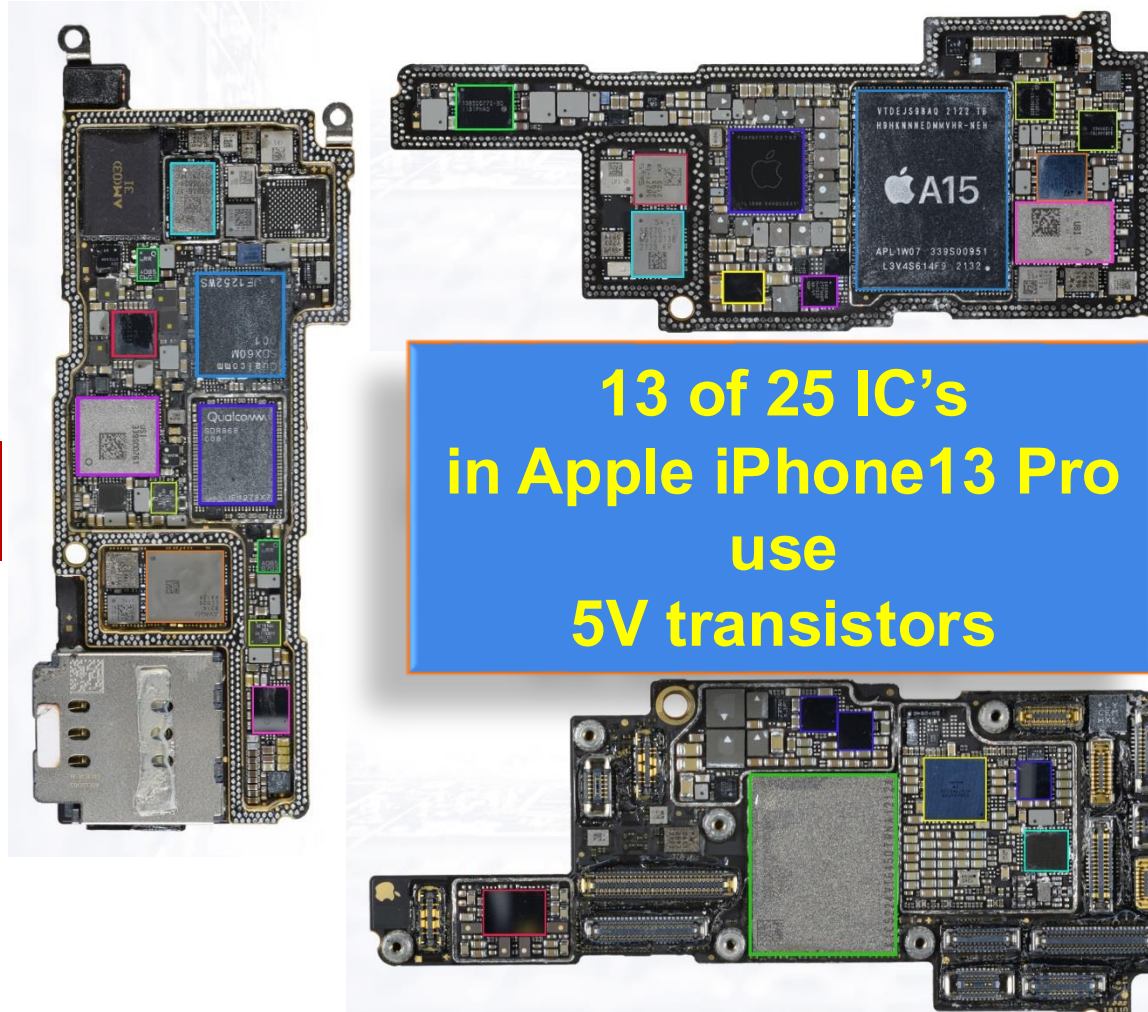


- ▶ **Targets higher voltage (5-40V) product area**
- ▶ **Strong customer demand for solutions**
- ▶ **MST brings significant improvement**
 - Early results showing gains in many areas
 - Allows manufacturers to shrink designs, cut product costs
- ▶ **Early stages of customer rollout**



$$L_{\text{DEVICE}} = 1.84\mu\text{m}$$

Example: Use Of 5V Transistor In Apple iPhone13



Qualcomm Snapdragon X60 5G Modem

Qualcomm RF Transceiver

USI Wi-Fi/BT Wireless Combo Module

Qualcomm PMX60 PMIC

STMicroelectronics Secure MCU/eSIM

Qorvo Envelope Tracker IC (2 pcs, likely)

Qualcomm Envelope Tracker IC

Avago Front-End Module

Broadcom Wireless Charging Receiver IC

Apple APL1W07 A15 Bionic PoP
(A15 AP + SK hynix 6GB LPDDR4X SDRAM)

Apple APL1098 PMIC

NXP Display Port Multiplexer

Skyworks SKY58271-19 Front-End Module

Skyworks SKY58270-17 Front-End Module

Apple/Dialog Semi 338S00770-B0 PMIC

Apple/Dialog Semi 338S00762-A1 PMIC

STMicroelectronics STB601A05 PMIC

USI Apple U1 UWB Module

Texas Instruments TPS65657B0 Display Power Supply

KIOXIA 256 GB NAND Flash

Apple/Cirrus Logic Audio Codec

NXP SN210 NFC & Secure Element

Apple/Cirrus Logic Audio Amplifier

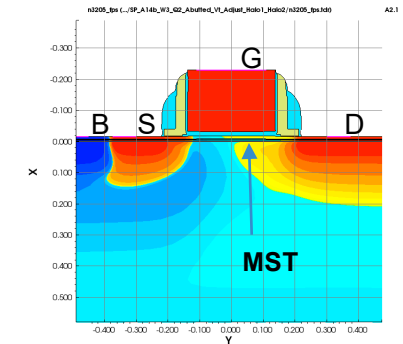
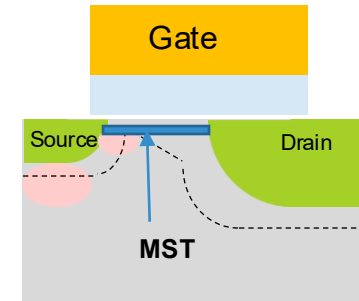
Apple/Cirrus Logic Power Conversion

- iPhone 13 Pro teardown by Tech Insights
- 5V transistor assessment by Atomera

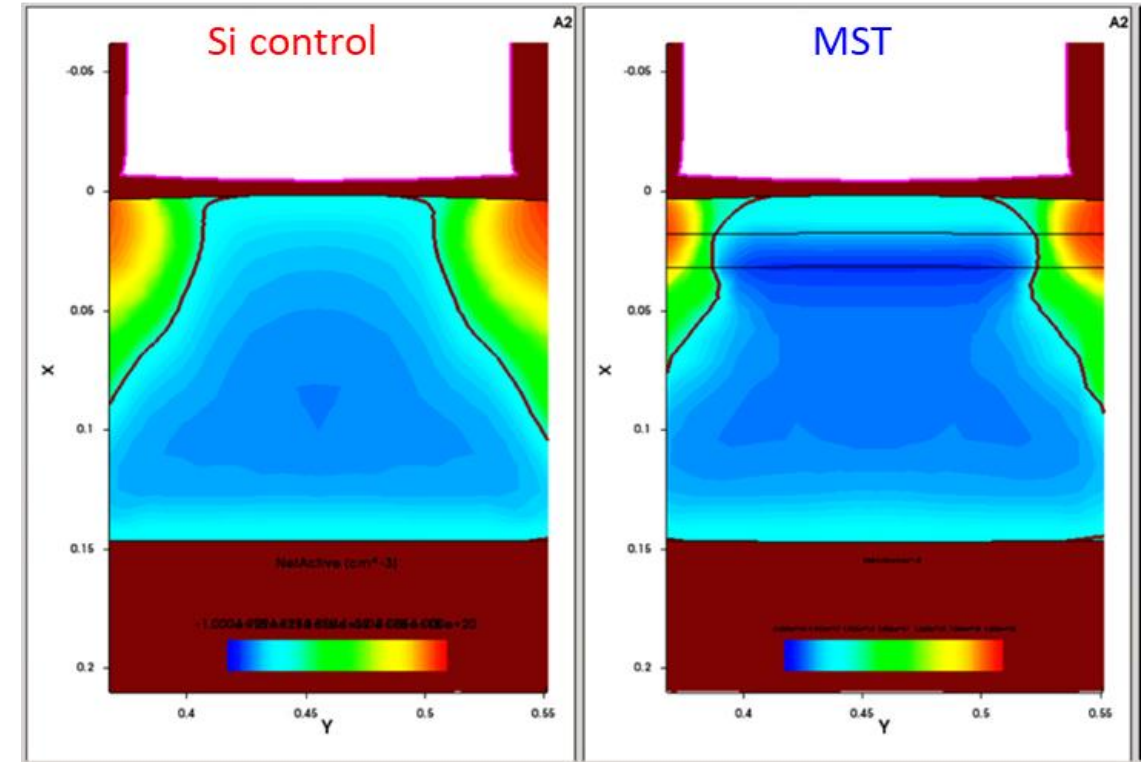
Reference https://www.techinsights.com/blog/teardown/apple-iphone-13-pro-teardown?utm_source=Prospect+Email&utm_medium=Email&utm_campaign=2021+-+Q3+-+Teardown+-+Blog+-+Apple+iPhone+13

5V MST-SP Product – Value Proposition

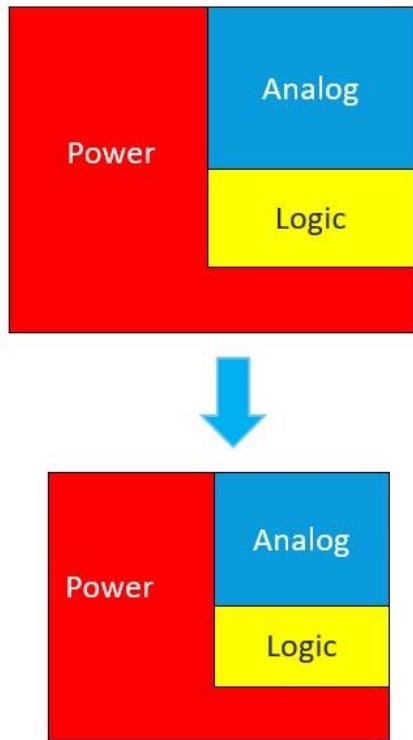
- ▶ **Industry best performance at 180nm (Rsp)**
 - Based on measured silicon data
 - Scalable to smaller process nodes
- ▶ **Meets all reliability requirements**
 - Breakdown Voltage (BVDSS) > 10.5V
- ▶ **Significant cost savings, performance benefits**
 - Die area reduction up to 20%
- ▶ **Demonstrates the big advantage MST can bring to highly optimized designs**
- ▶ **Complete design package accelerates time to production**



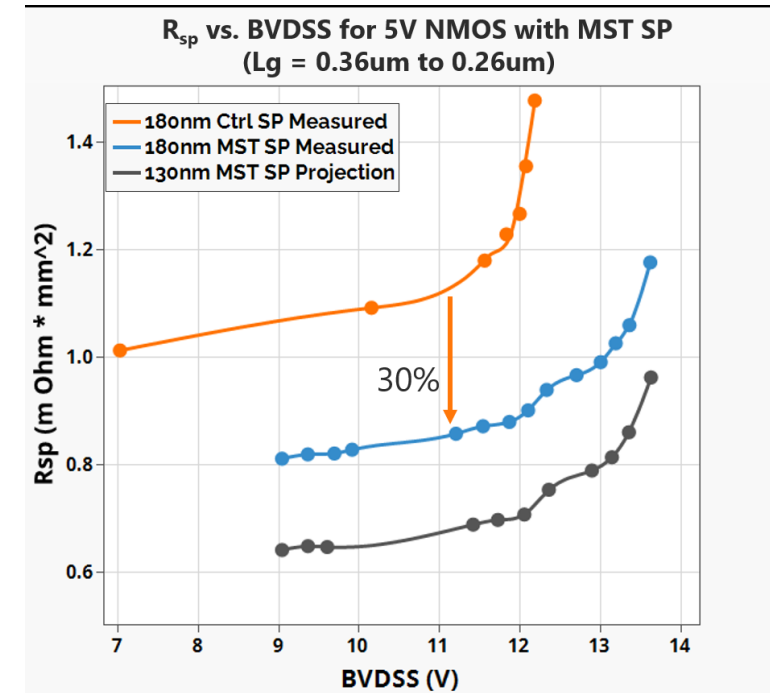
- ▶ **Leading semiconductor companies use TCAD to model manufacturing processes**
 - MSTcad is an add-on for MST
- ▶ **MSTcad can speeds up the time needed to evaluate multiple MST integration options**
- ▶ **Lowers cost of MST evaluation**
- ▶ **Speeds time to successful wafer runs**
- ▶ **Fewer wafer runs lead to faster production**



MST enables legacy capacity expansion

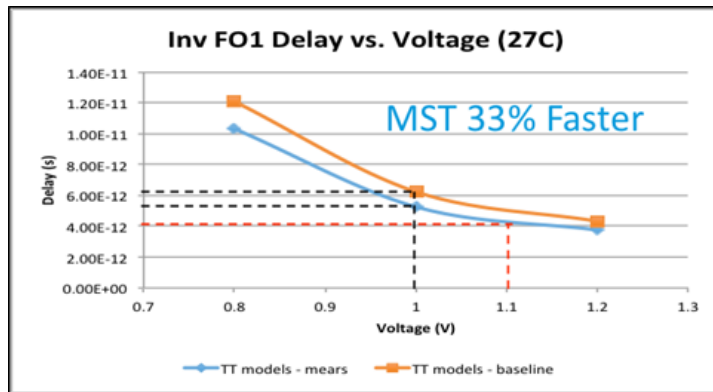


- ▶ **MST provides 30% performance advantage**
 - 0.13u analog design
 - MST vs control silicon
- ▶ **Enables a die shrink of 15-20%**
- ▶ **Smaller die means more manufacturing capacity**
 - Without the cost of building a new fab



MST 28nm benefits

MST shows 30% higher performance



MST performance improvement due to:

- Higher electron mobility
- Improved gate oxide integrity enabling higher overdrive

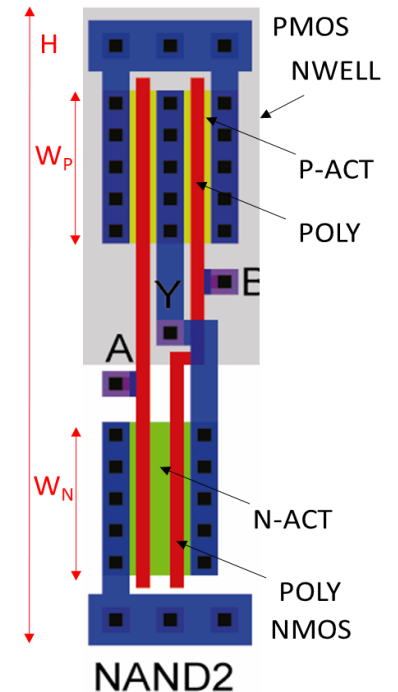
► Performance improvements due to MST can be traded for area reduction

► 28nm PDK SPICE model used to showcase:

- Logic scaling with MST shows 22-25% area reduction
 - Using a NAND2 gate
- Analog scaling with MST shows up to 21% area reduction

► Implementation of MST on new 28nm designs can result in >20% more production capacity

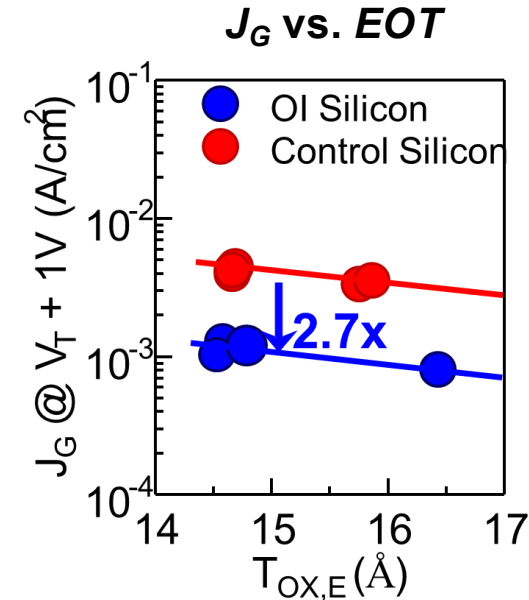
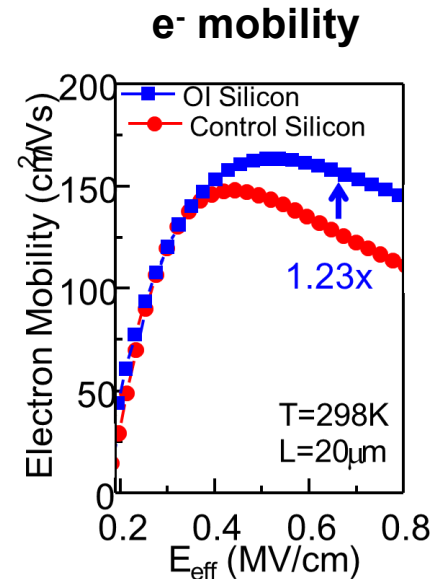
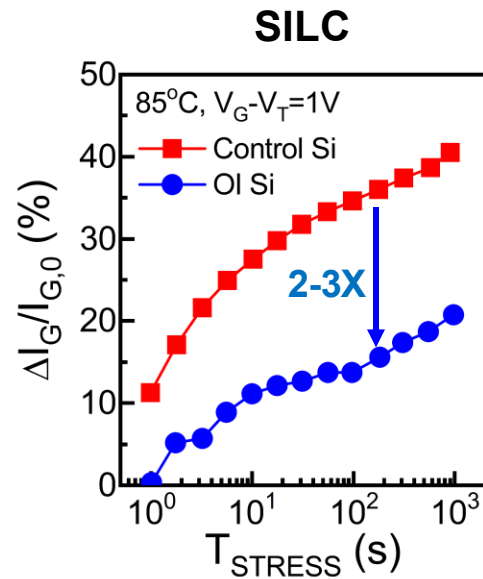
► Allows excellent economic benefits for the whole value chain



MST for High-k metal gate (HKMG) transistors

► MST enhances HKMG transistor performance and reliability*

- Reduced stress induced leakage current (SILC) enabling reliability improvement
- 23% long-channel mobility enhancement
- 2.7x lower gate leakage



* Professor Suman Datta Group

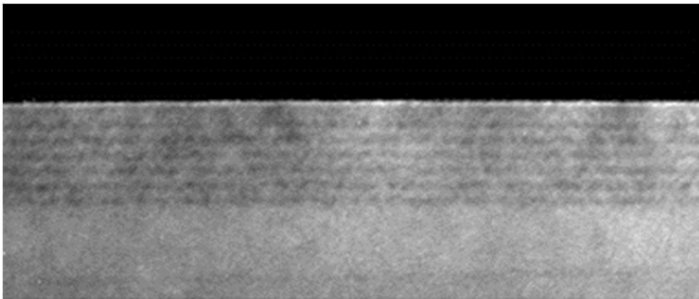


MST: Mears Silicon Technology



Quantum Engineered Silicon

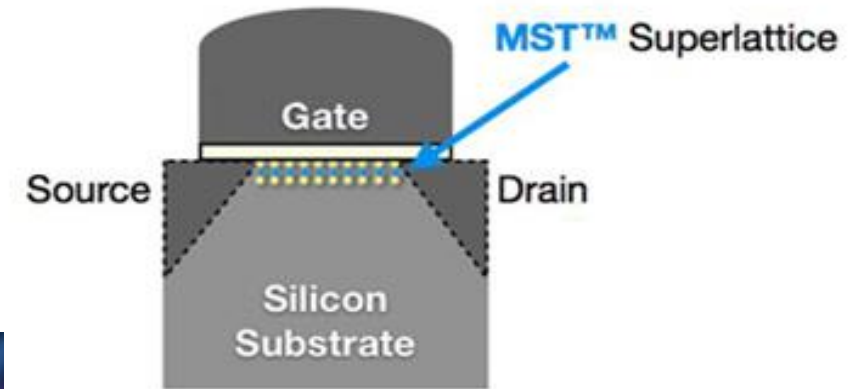
Partial Monolayers of Oxygen in Silicon



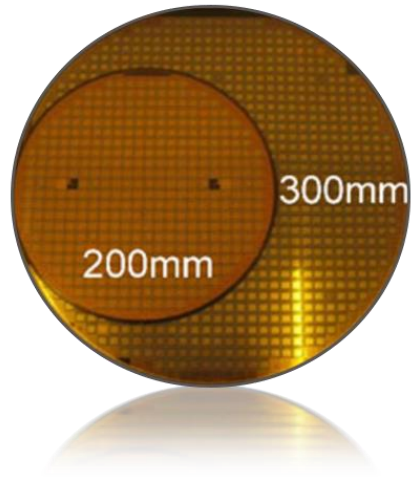
Supported by
Major Semiconductor
Tool Suppliers



MST Enhanced Transistors



Atomera state of the art research center



Epi Deposition Tool

► Epi deposition facility

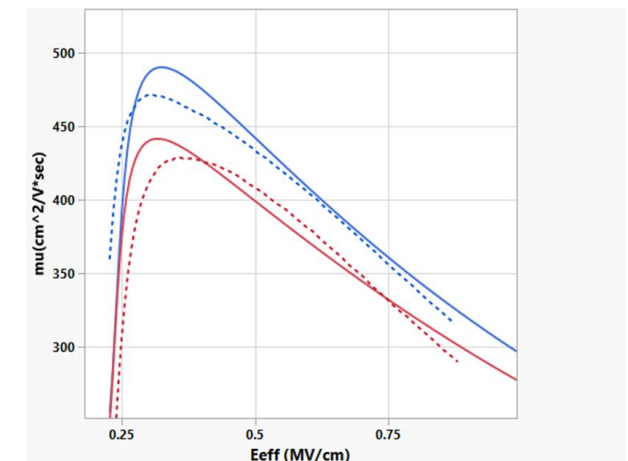
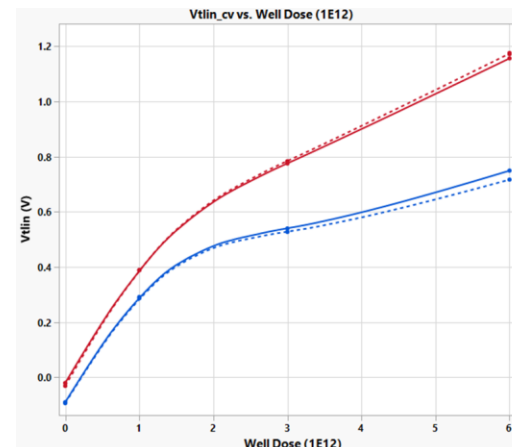
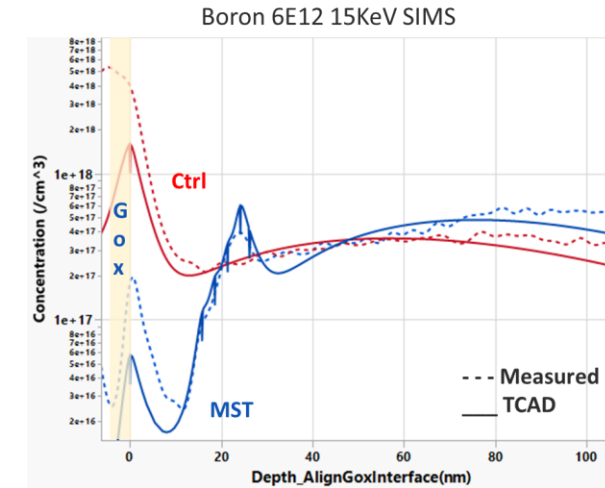
- 300mm Epi deposition
- 200mm Epi deposition
- Wafer cleaning equipment
- Metrology tools
- Advanced wafer handling
- World class clean room facility

► Available to deliver customer wafers

Atomera MSTcad™ Progress



- ▶ Leading semiconductor companies use TCAD
- ▶ MST is modelled with a TCAD add-on called MSTcad
- ▶ These plots show silicon verification of MSTcad simulations
- ▶ Enables good electrical match-up for 5V NMOS and MST SP
- ▶ Should speed time to successful results with customers



MST1 vs MST2

► MST1

- Blanket technology
- Easy to integrate
- Deposited at beginning of mfg process
- Degraded by high heat in STI/Well module
- Faster time to market for low heat processes
- Used for FinFET, RFSOI, newer process nodes

► MST2

- Selective technology
 - Integrated after STI/Well so avoids highest heat
- More flexible to apply to selected areas only
- Used for 5V, Analog, older process nodes

Wafer manufacturing process

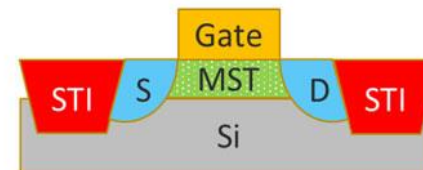
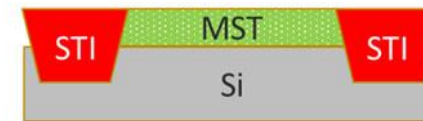
Blank Si wafer

Shallow Trench Isolation (STI) & Well module

Gate module

Source/Drain module

MST1



MST2

