



Andes Technology Corp.

2026 Investor Conference

June 3rd 2026

Safe Harbor Notice



Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.



Topics

- | **Company Introduction**
- | **The Financial & Operation Results**
- | **Target Major Applications**
- | **The R&D Power for The Future**

Company Introduction

(TWSE: 6533)

Andes HQ New Office



Company Introduction

Highlights

- **Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.**
- **Well-established high technology IPO company**
- **Around 500 people; 80% are engineers.**
- **TSMC OIP Award “Partner of the Year” for New IP (2015)**
- **Founding Premier membership in the RISC-V International Association (RISC-V Foundation) (2020)**
- **AI Global Media Award “Most Outstanding Embedded Processor IP Supplier” (2020)**
- **EE Awards - “Taiwan-Product Award” & ”Asia-Company Award” (2021)**
- **Top 500 High-Growth Companies Asia-Pacific (2023)**

Mission

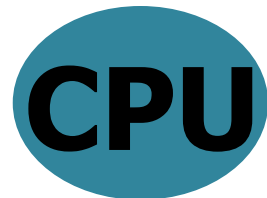
- **Innovate performance-efficient processor solution for low-power SoC**

Emerging Opportunities

- **Smart and Green electronic devices**
- **Cloud Computing and Internet of Things and Machine Learning**

Andes Technology Corp.

Who We Are



Pure-play CPU IP Vendor

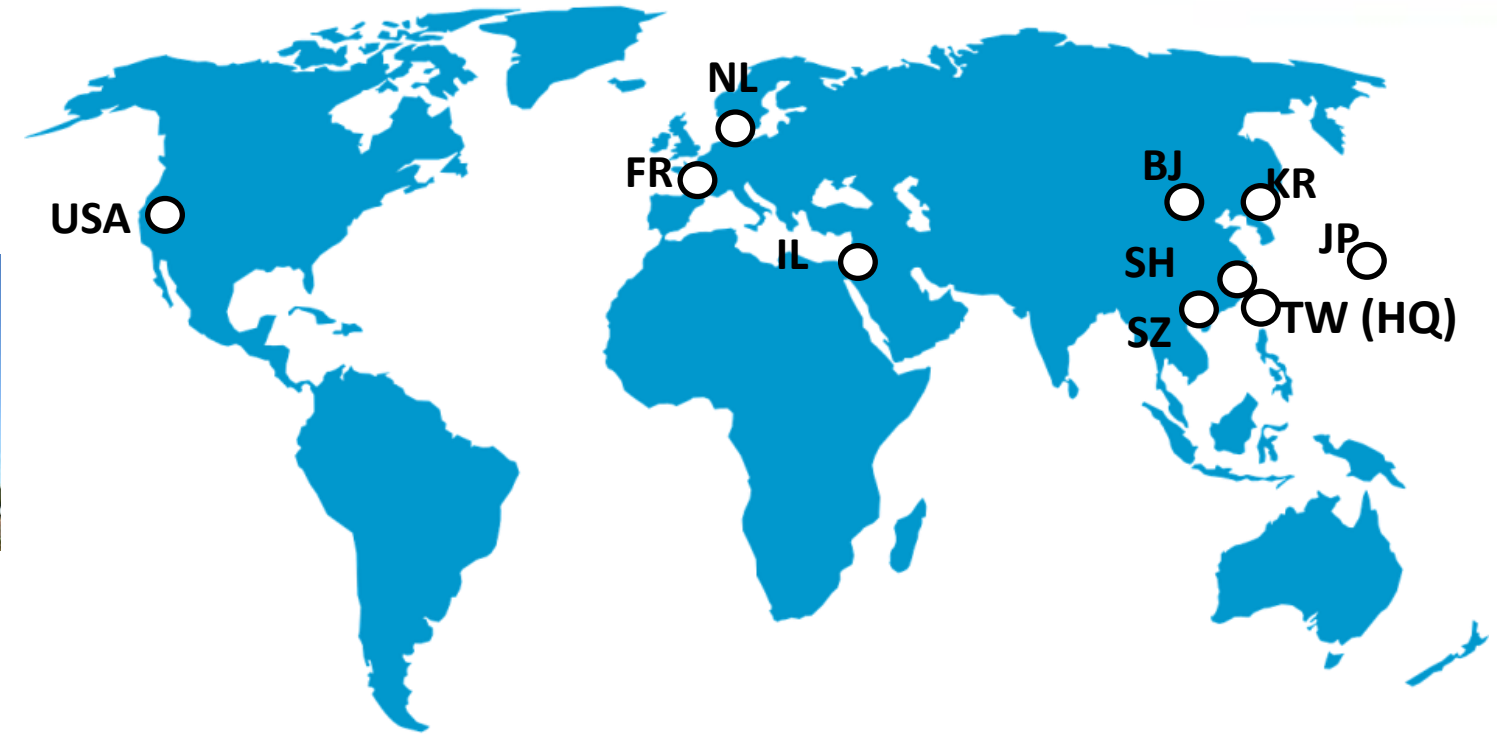


20-year-old
Public Company



Active Open-Source Contributor/Maintainer

Hsinchu, TW (HQ)



Active Roles in RISC-V Community



Founding & Premier Member

- Director of the Board
- Technical Steering Committee
- Chair/Co-Chair of Task Groups



Founding and Premier Member

- Governing Board
- Technical Steering Committee

Quick Facts

5th gen architecture
AndeStar™ V5, RISC-V
adopted

400⁺
Employees, 80% R&D

350⁺
Worldwide
Licensees

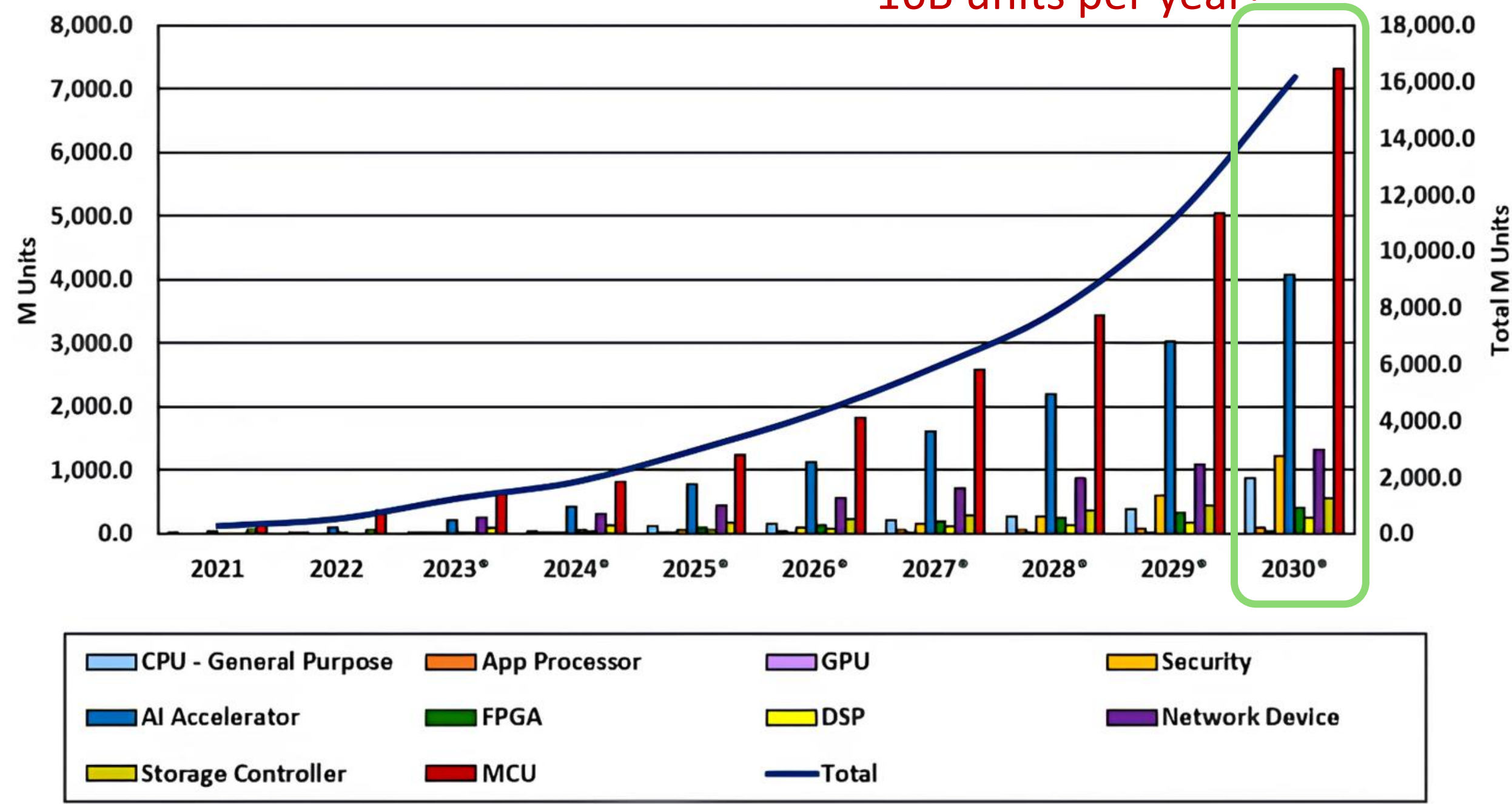
~100K
AndeSight IDE
installations

~20Bn⁺
Total shipment of
Andes-Embedded™ SoC

Chip Shipped Forecast on RISC-V Worldwide

SHD Group Market Report

By 2030 it will be over
16B units per year!



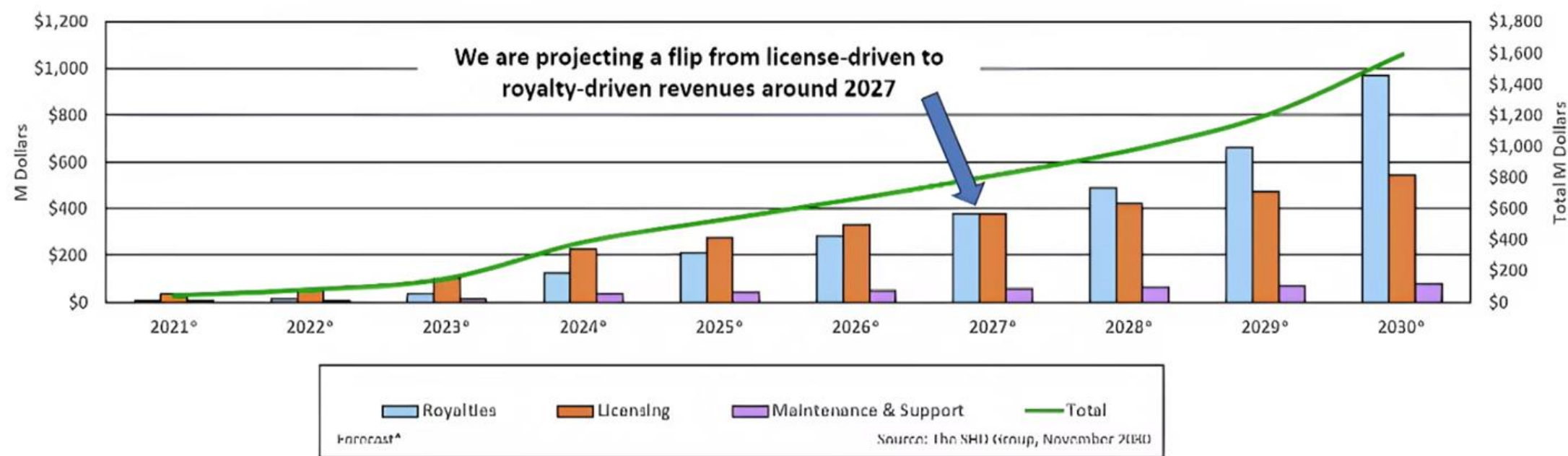
*Forecast

Source: The SHD Group, January 2024

Projected Andes' RISC-V Market Share

SHD Group Market Report

RISC-V IP Market Revenues to Grow



We estimate Andes currently has over 30% SOM by unit volume

RISC-V vendors in shipping SoCs

- Andes Technology
- Codaip
- DIY (home grown RISC-V)
- SiFive
- T-Head

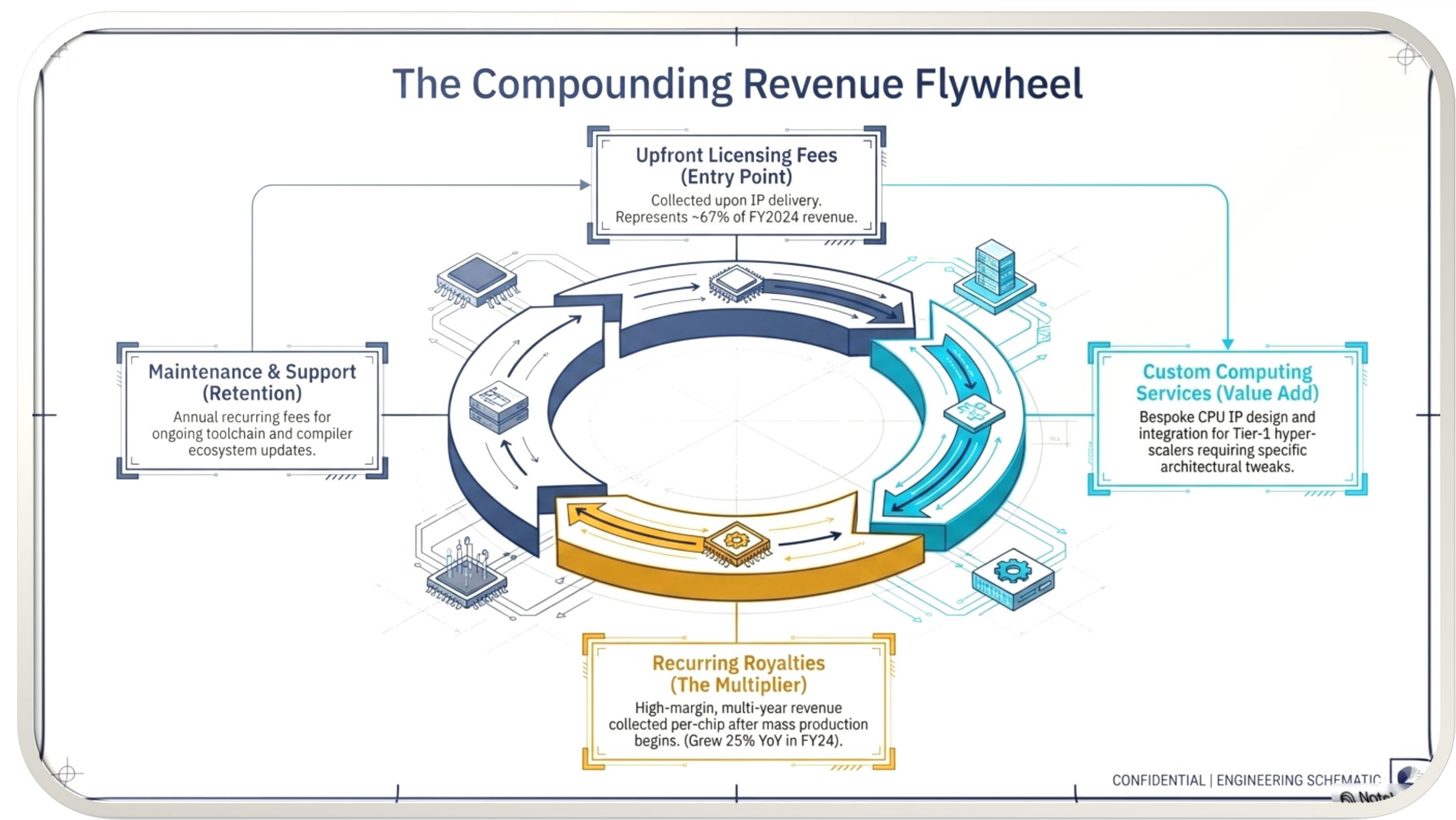
New sources of RISC-V IP expanding the market

- Imagination Technologies
- Synopsys
- Tenstorrent
- Ventana Microsystems
- others

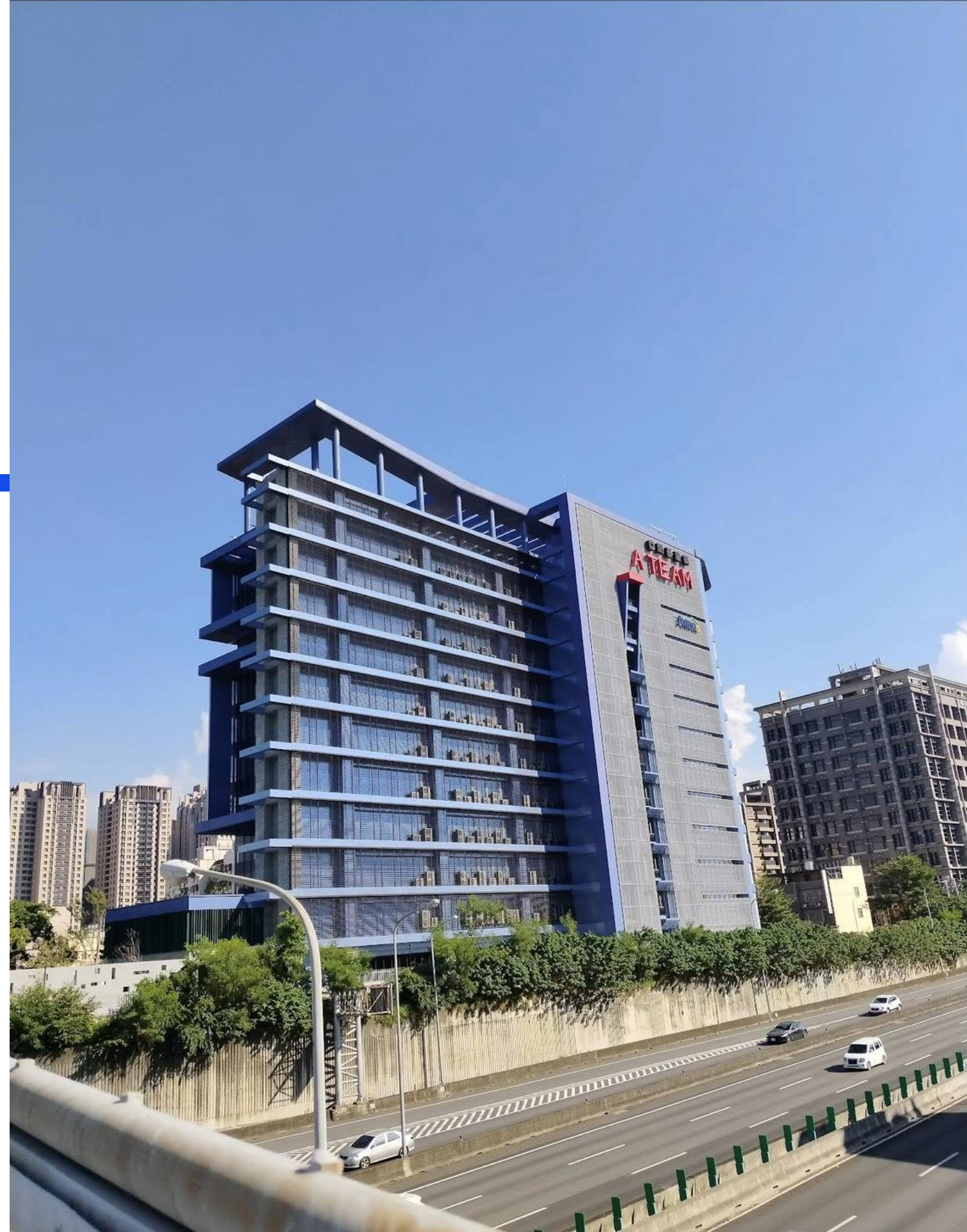
the SHDgroup

“Andes Technology, with its profound technological accumulation, comprehensive product lines, and excellent customer service, holds an important position in the global RISC-V CPU IP market. With the vigorous development of the RISC-V ecosystem, Andes Technology's market share is expected to continue to grow, becoming a key force in promoting industrial innovation.”

Business Model



The Financial & Operation Results



Monthly Revenue for 2025

Unit: TWD in Thousand

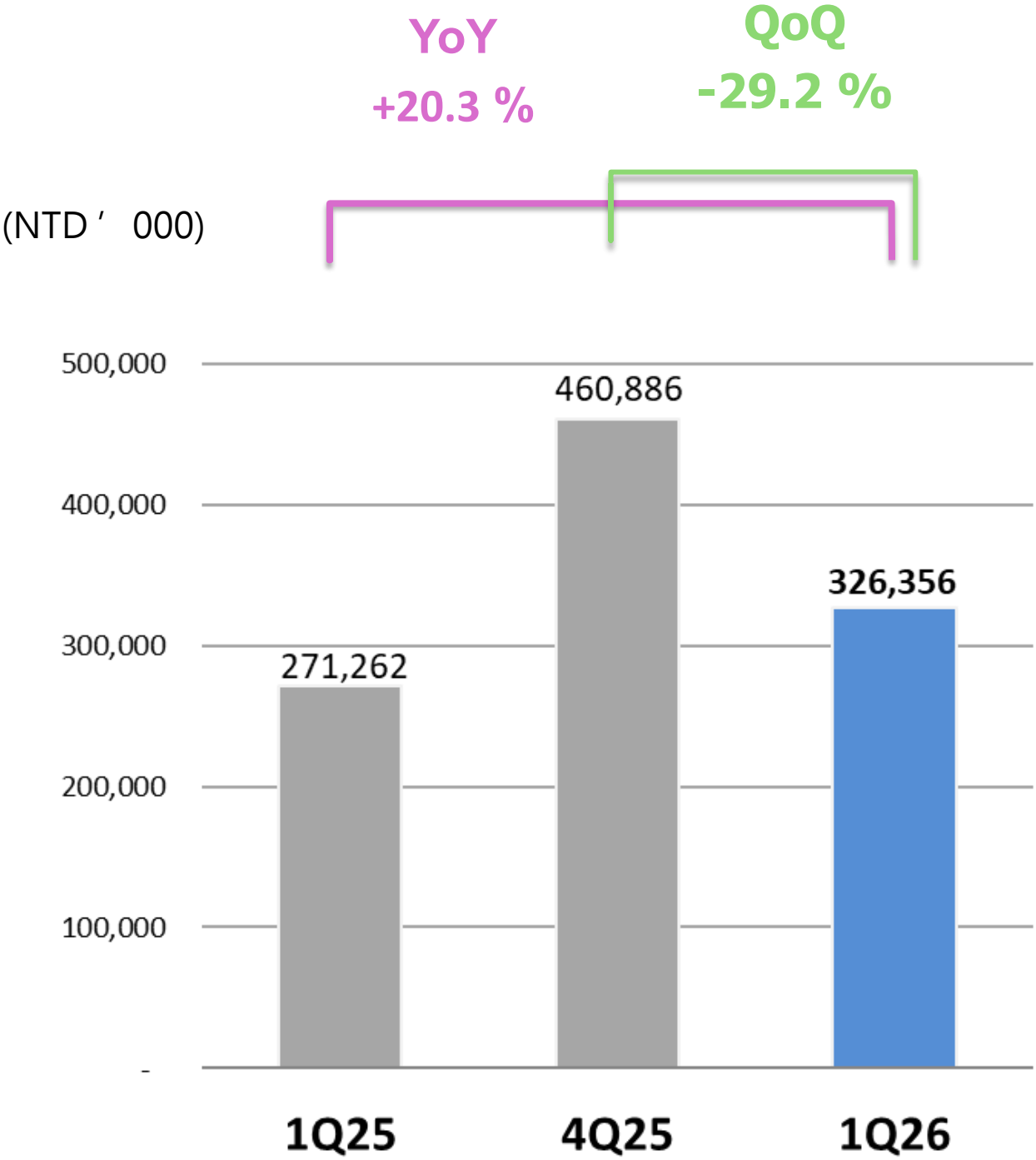
Year	Month	Operating Revenue			Accumulated Operating Revenue		
		current year	preceding year	Increase (Decrease) (%)	As of The End of This Month In Year	The Corresponding Period	Increase (Decrease) (%)
2025	12	201,051	155,847	29.01%	1,478,187	1,381,507	7.00%
2025	11	109,458	152,257	-28.11%	1,277,136	1,225,660	4.20%
2025	10	150,377	153,204	-1.85%	1,167,678	1,073,403	8.78%
2025	9	214,636	233,249	-7.98%	1,017,301	920,199	10.55%
2025	8	153,503	79,221	93.77%	802,665	686,950	16.84%
2025	7	98,395	116,159	-15.29%	649,162	607,729	6.82%
2025	6	107,240	47,852	124.11%	550,767	491,570	12.04%
2025	5	85,291	95,132	-10.34%	443,527	443,718	-0.04%
2025	4	86,974	135,448	-35.79%	358,236	348,586	2.77%
2025	3	95,726	85,785	11.59%	271,262	213,138	27.27%
2025	2	80,040	50,523	58.42%	175,536	127,353	37.83%
2025	1	95,496	76,830	24.30%	95,496	76,830	24.30%

Monthly Revenue for the Past 12 months

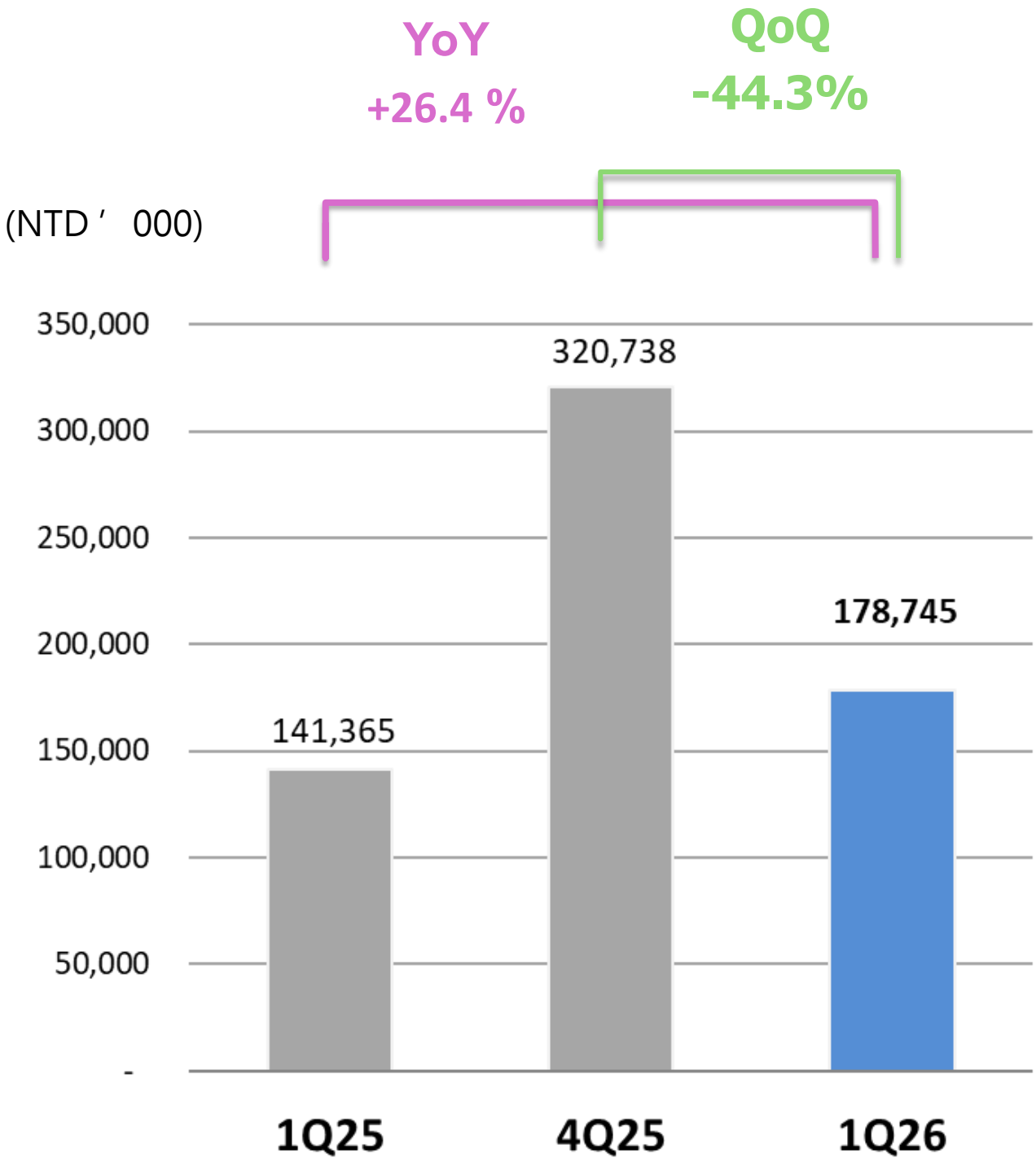
Unit: TWD in Thousand

Year	Month	Operating Revenue			Accumulated Operating Revenue		
		current year	preceding year	Increase (Decrease) (%)	As of The End of This Month In Year	The Corresponding Period	Increase (Decrease) (%)
2026	4	106,862	86,974	22.87%	433,218	358,236	20.93%
2026	3	133,545	95,726	39.51%	326,356	271,262	20.31%
2026	2	89,855	80,040	12.26%	192,811	175,536	9.84%
2026	1	102,956	95,496	7.81%	102,956	95,496	7.81%
2025	12	201,051	155,847	29.01%	1,478,187	1,381,507	7.00%
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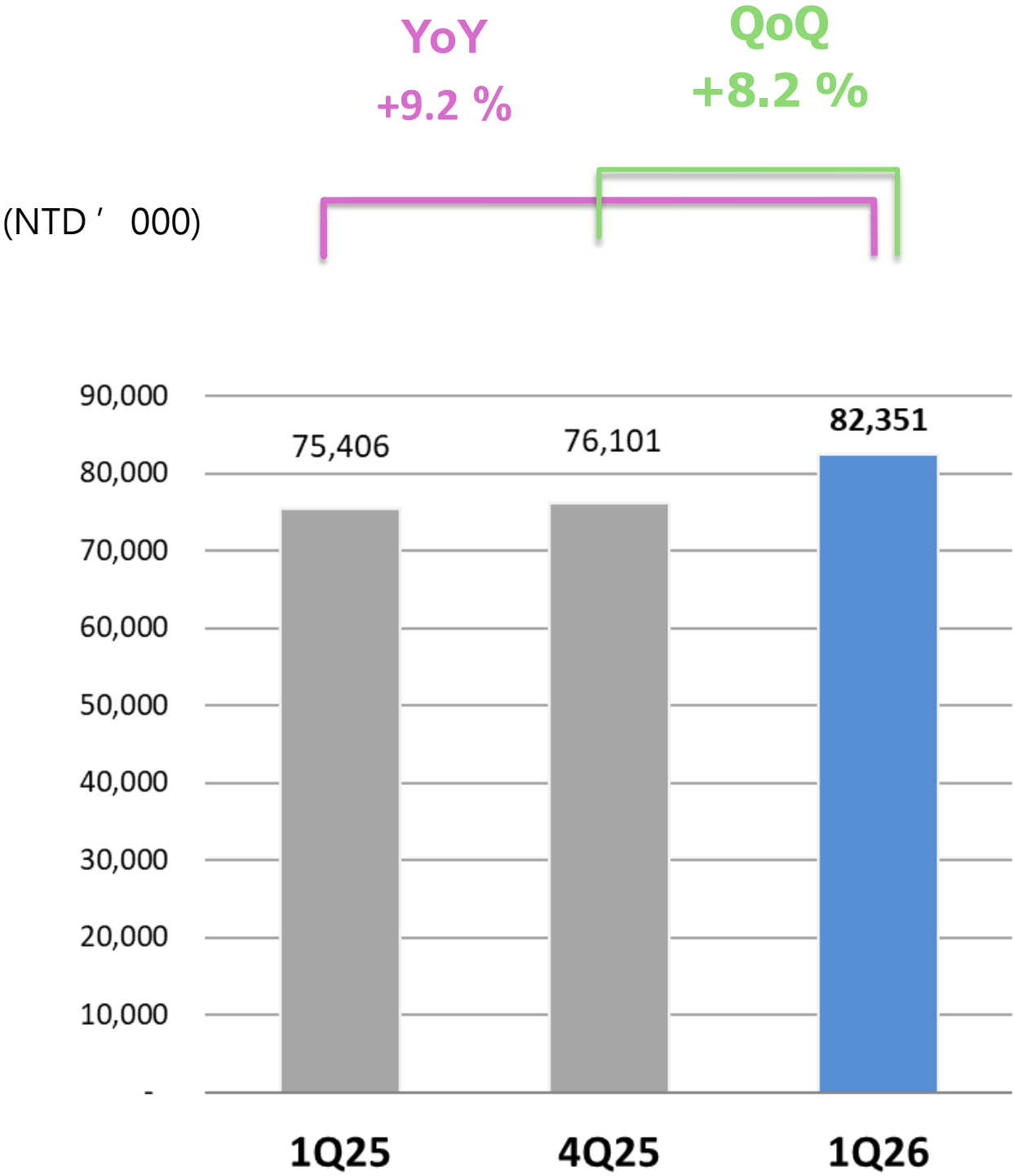
1Q26 Revenue Analysis



1Q26 License Analysis



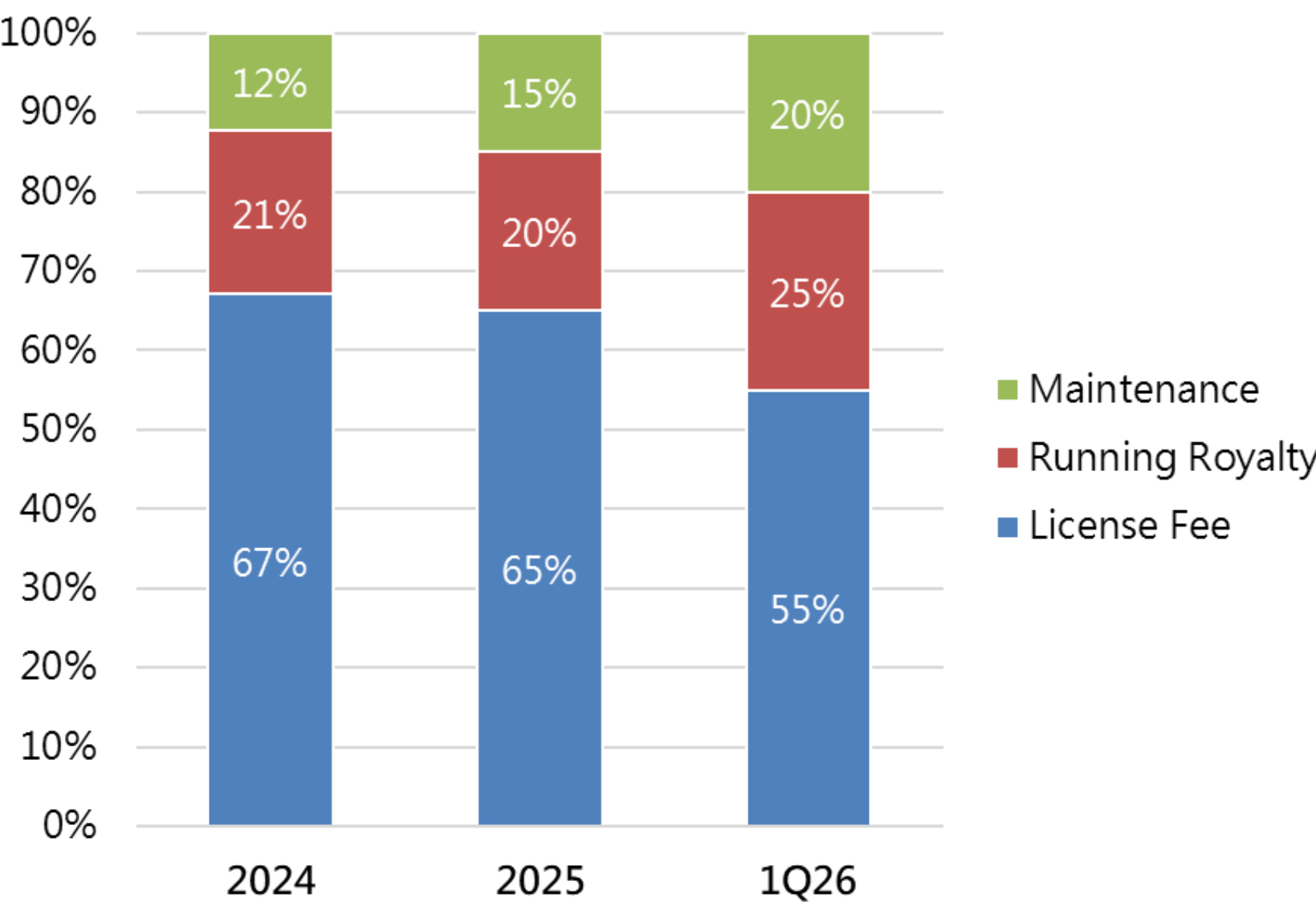
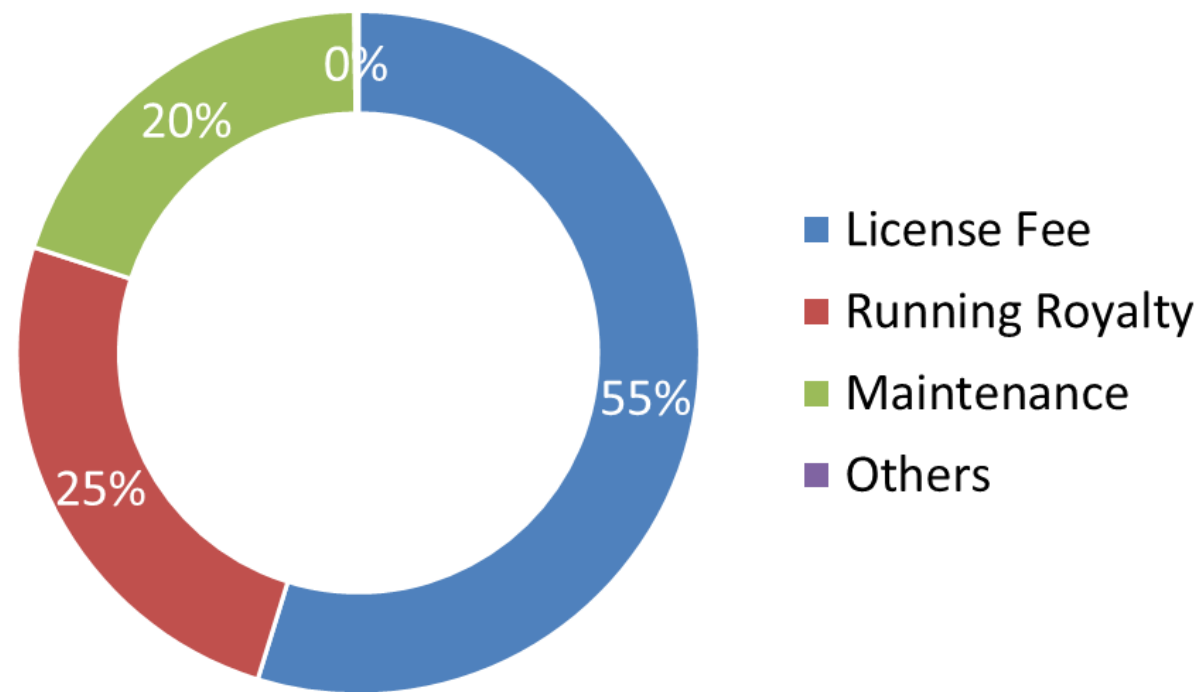
1Q26 Royalty Analysis



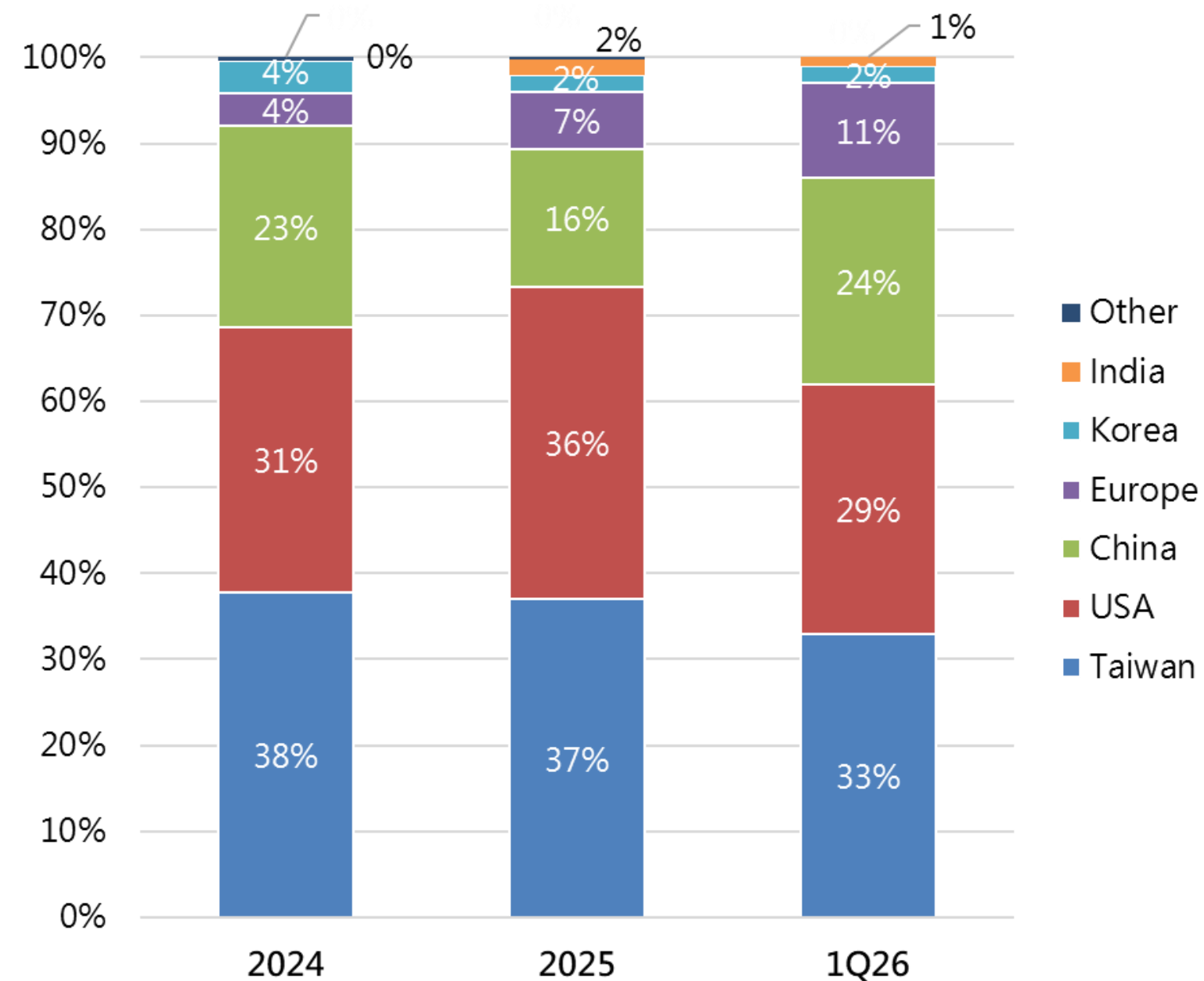
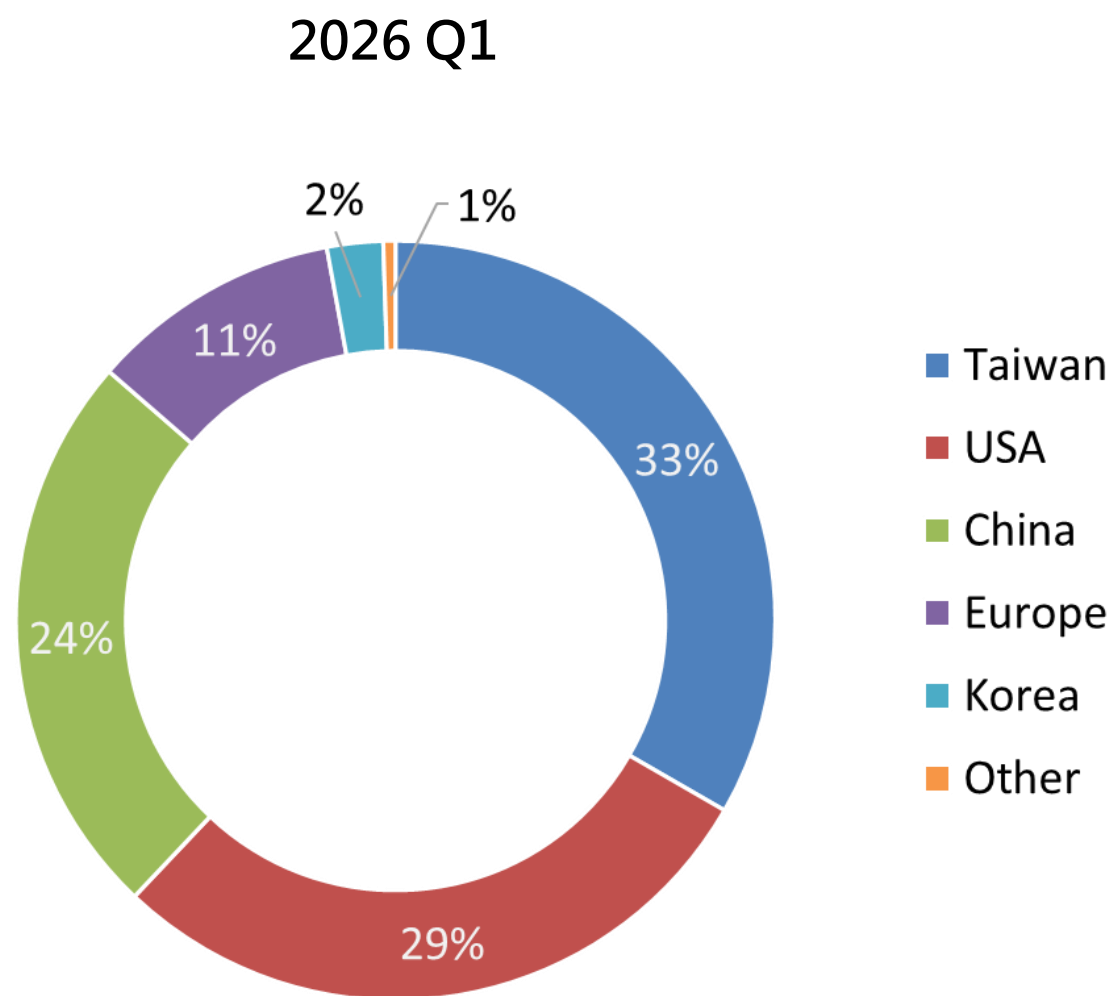
1Q26 Revenue Analysis by Business Model



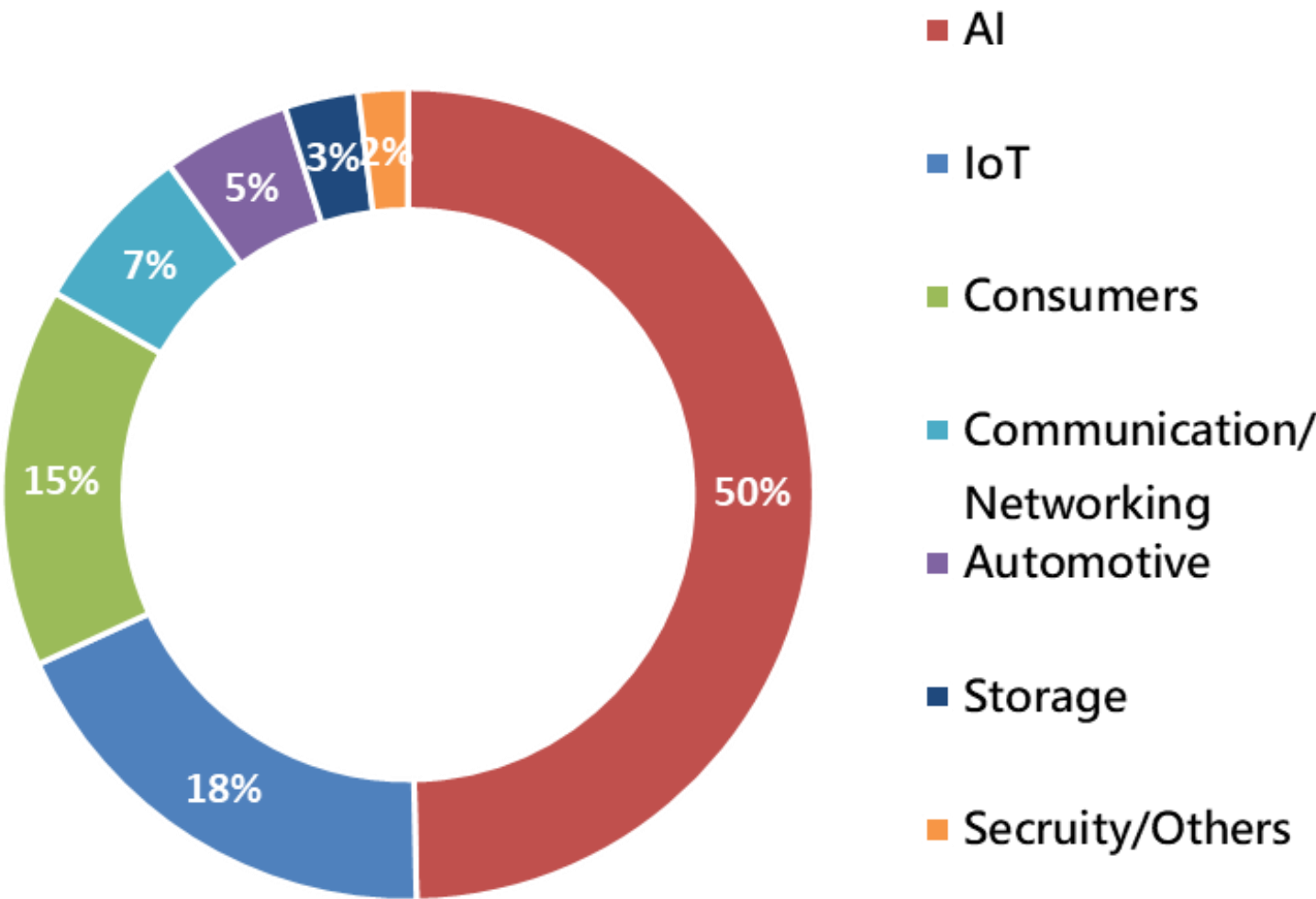
2026 Q1



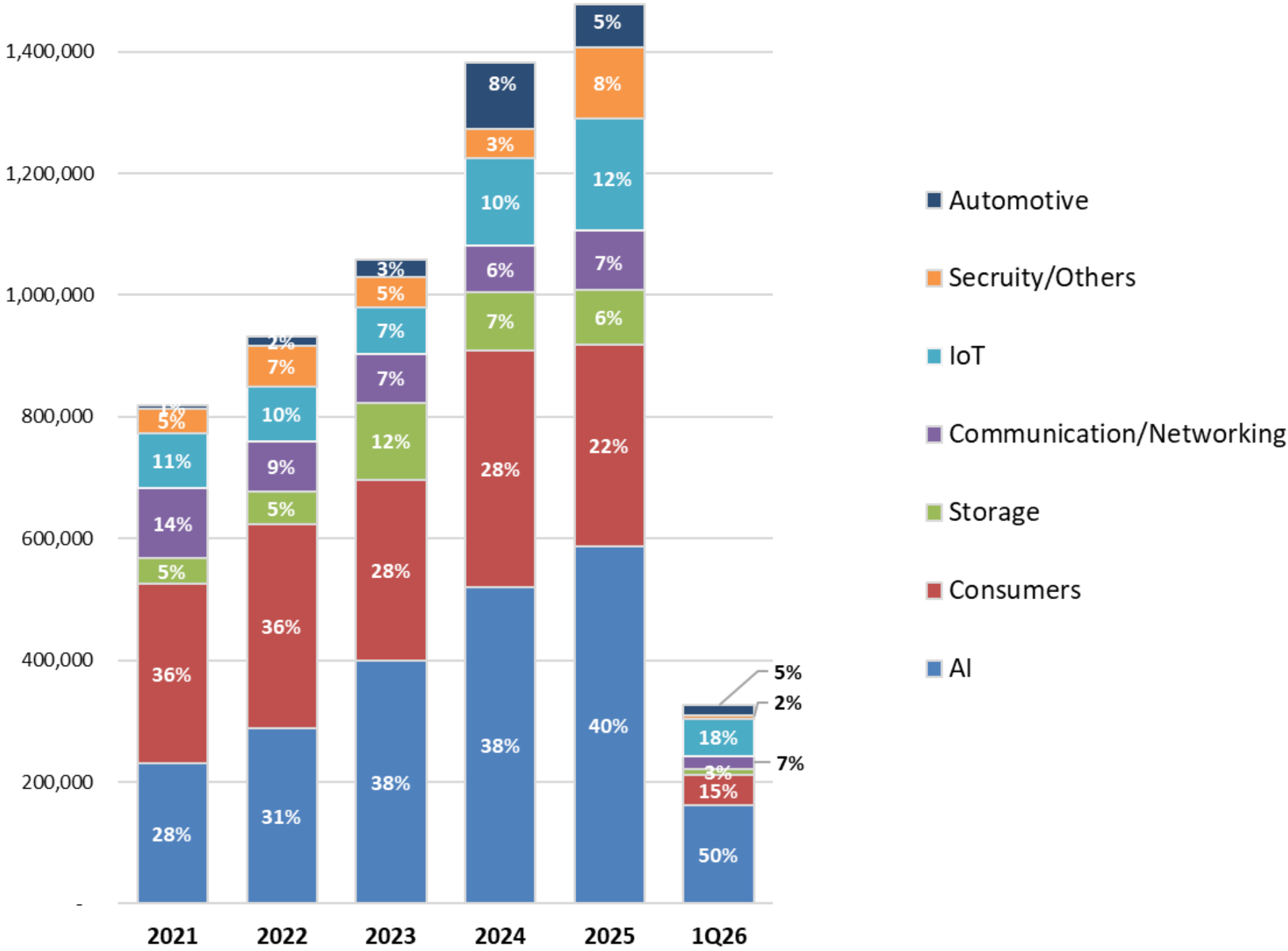
1Q26 Revenue Analysis by Region



1Q26 Revenue Analysis by Application



2021 to 1Q26 Revenue Analysis by Application

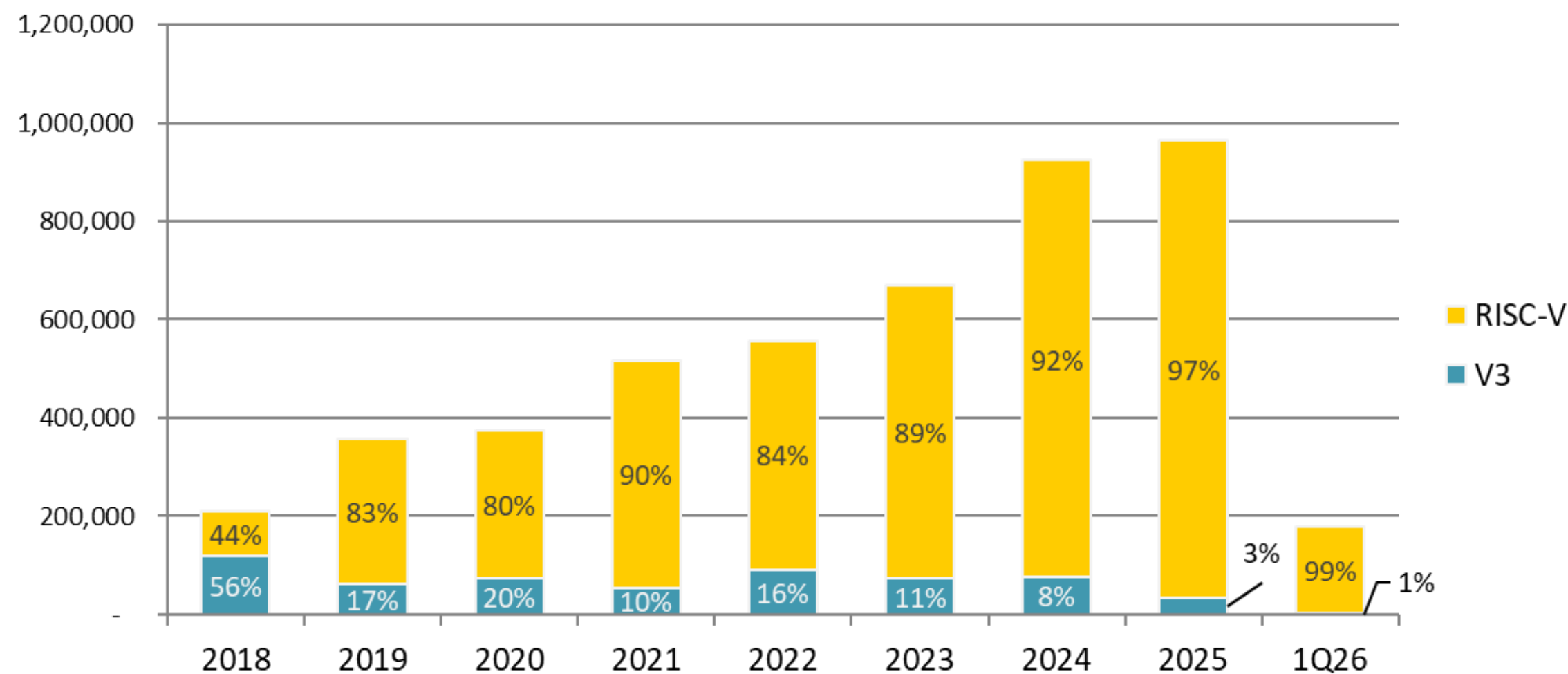


Historical License Revenue Analysis



License Revenue

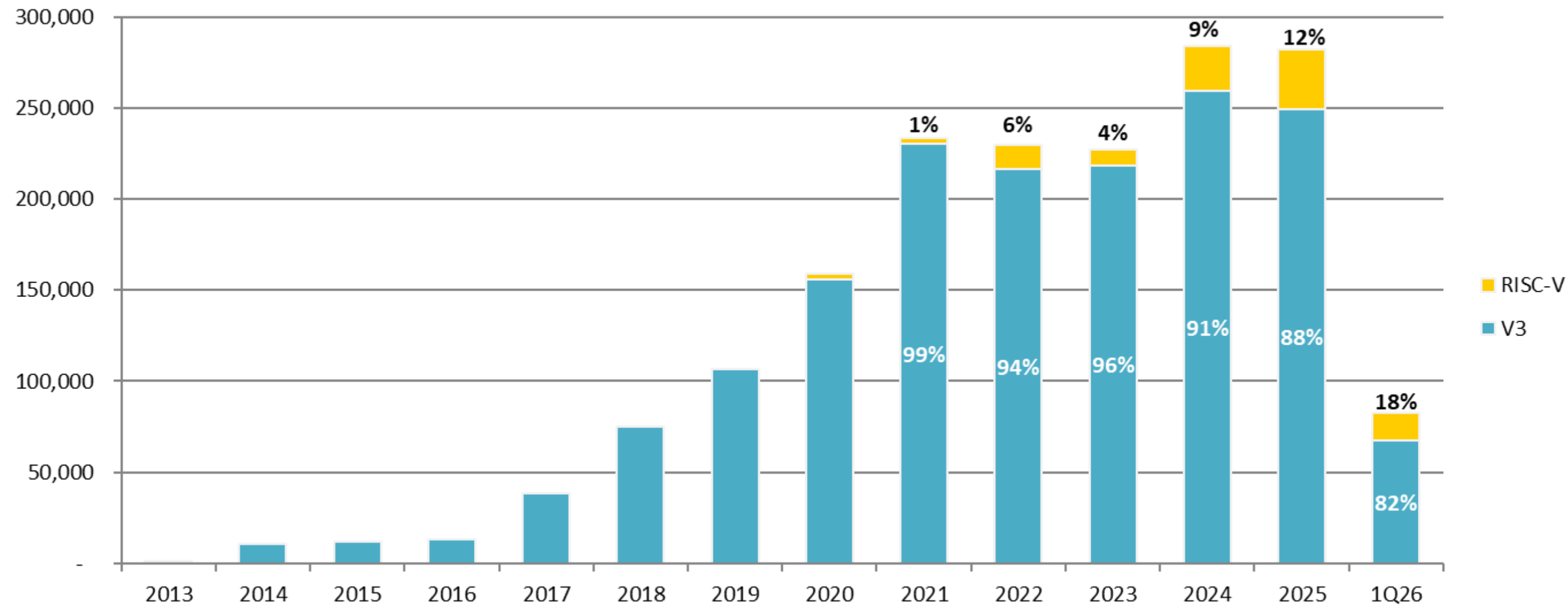
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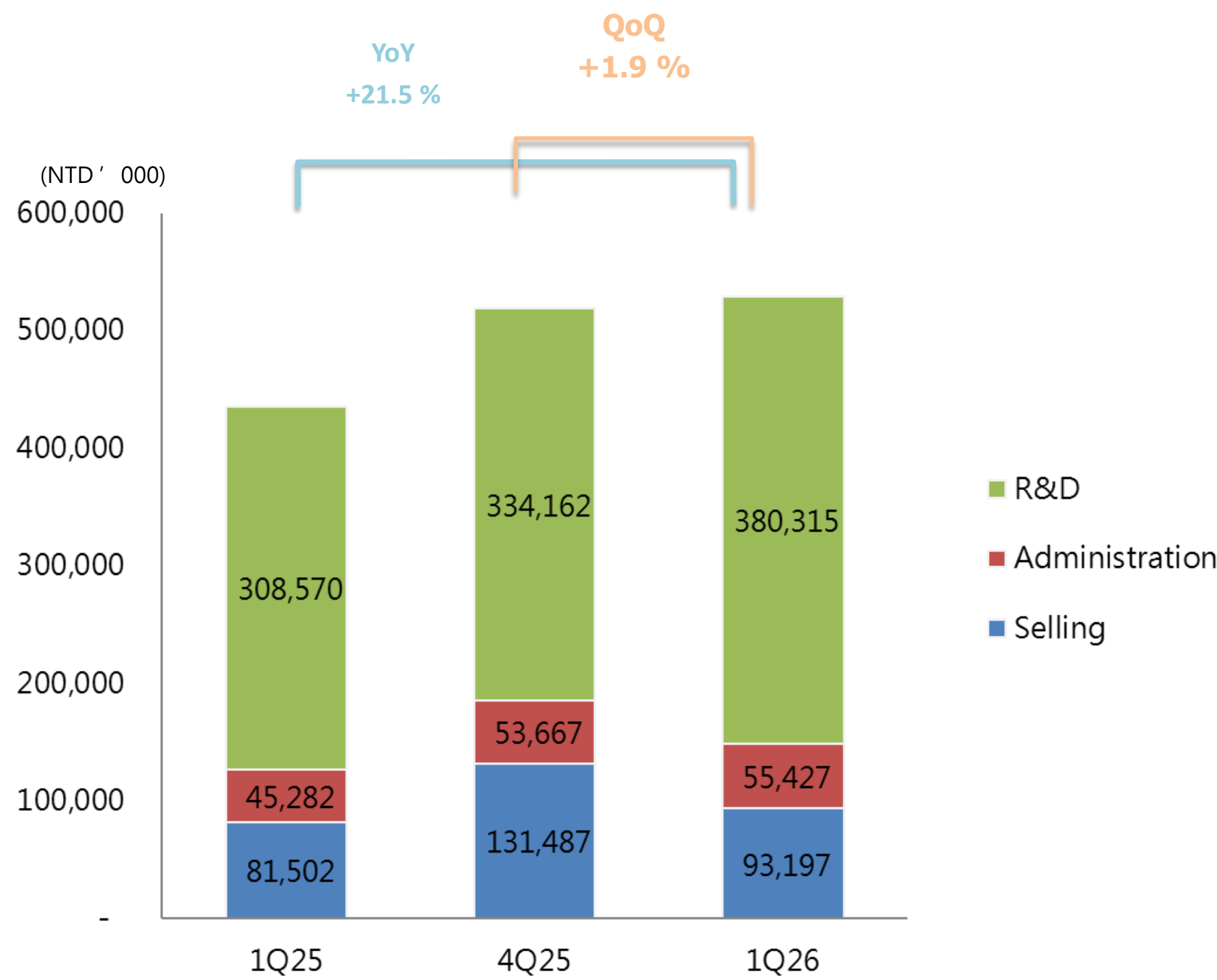
Historical Royalty Revenue Analysis

Royalty Revenue

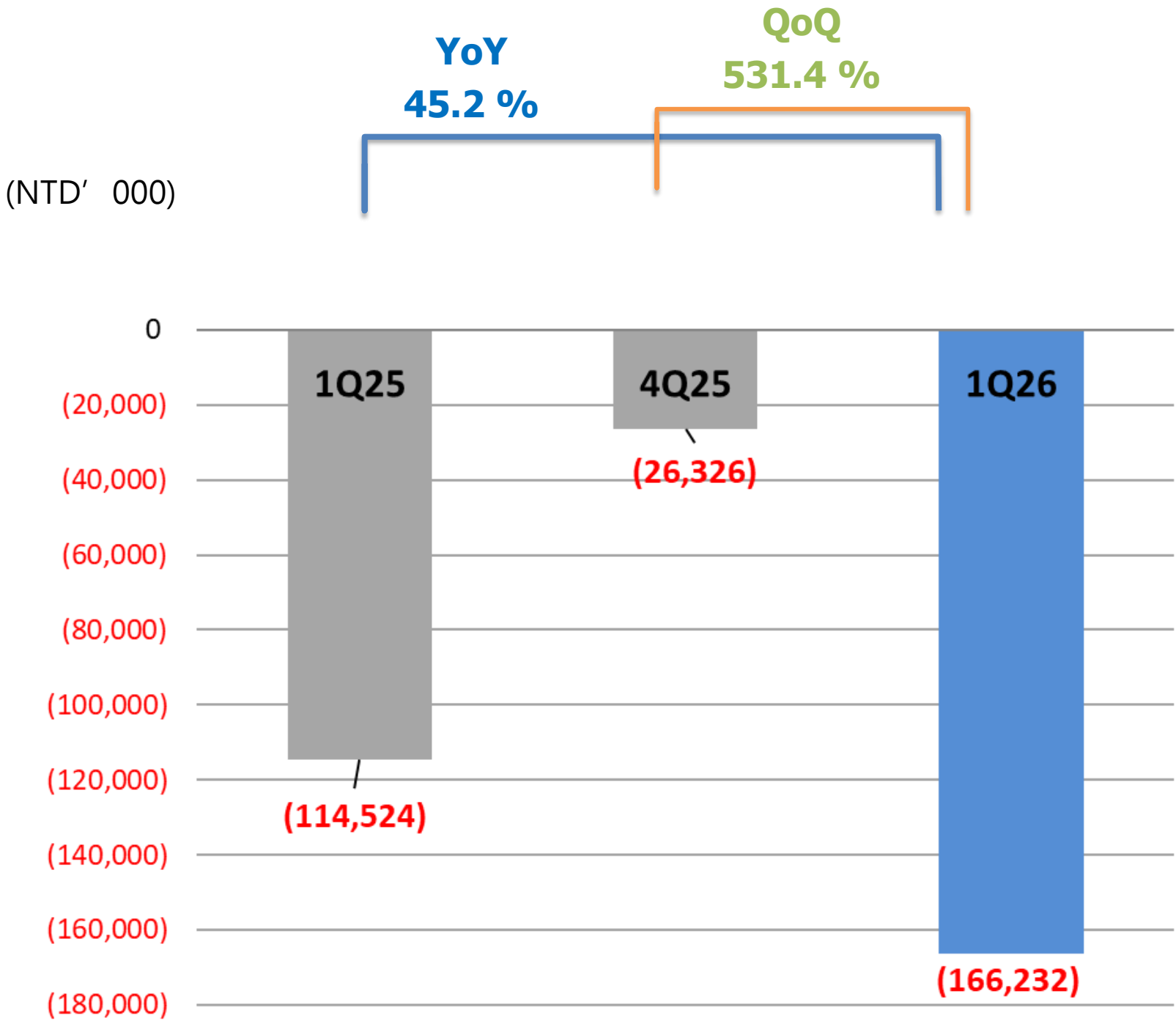
(NTD ' 000)



2026 Q1 Operating Expense Analysis



2026 Q1 Net Income (Loss) Analysis



2026 Q1 EPS: (3.28)
2025 Q4 EPS: (0.52)
2025 Q3 EPS: 0.17
2025 Q2 EPS: (5.58)
2025 Q1 EPS: (2.26)

Key Applications and the Trend



The Key Applications & The Trend



The global Automotive market size was valued at USD 341255.0 million in 2024 and is expected to expand at a **CAGR of 16.4%** during the forecast period, reaching USD 848836.0 million by 2031.

RISC-V will capture 10% of the Automotive market by 2025
Counterpoint, Sept 2021



The global Internet of Things (IoT) market size is projected to grow from \$714.48 billion in 2024 to \$4,062.34 billion by 2032, at a **CAGR of 24.3%...**

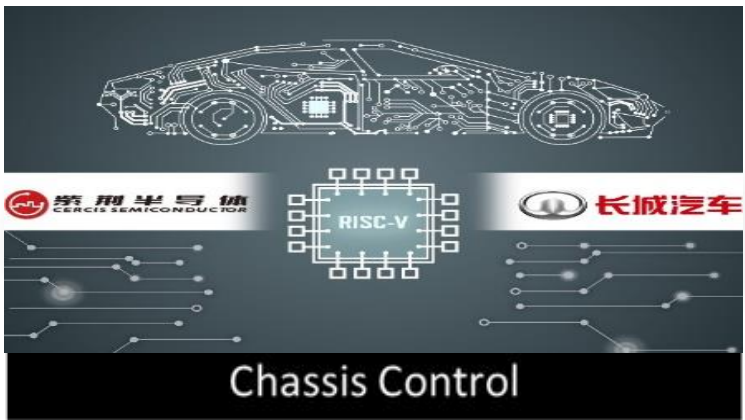
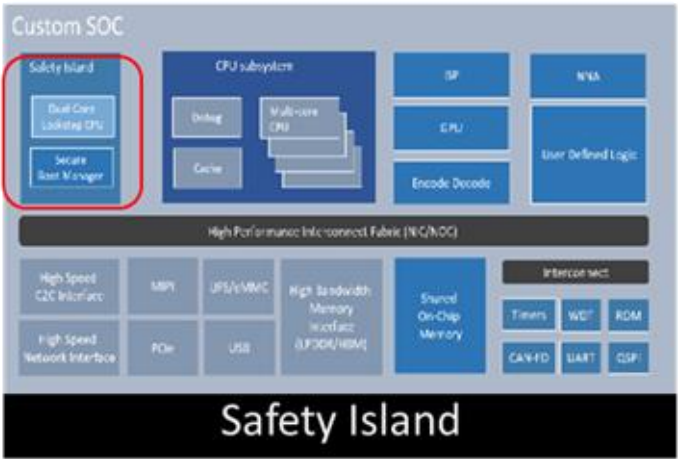
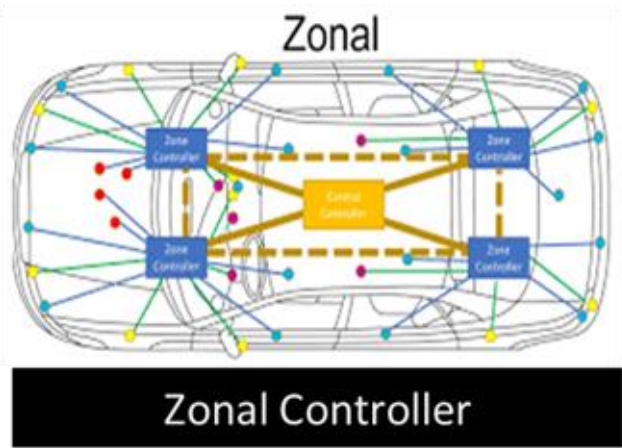
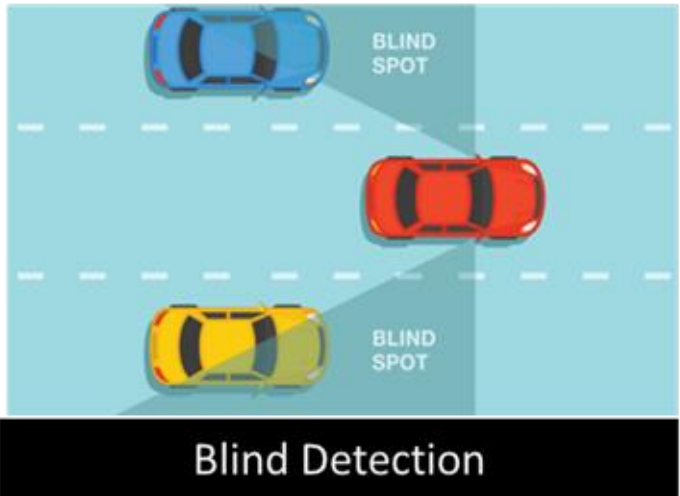
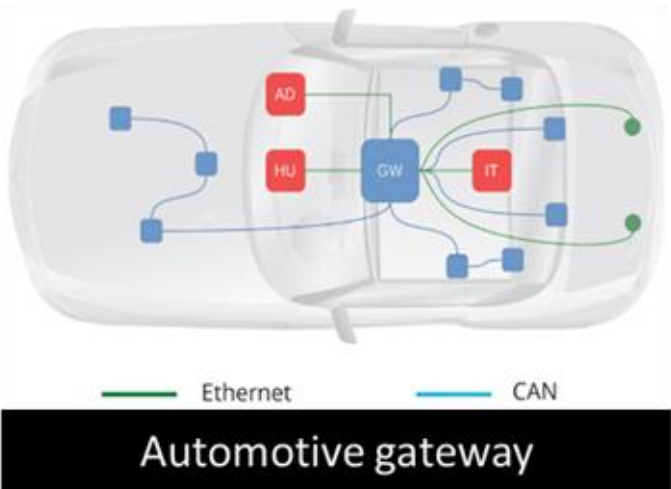
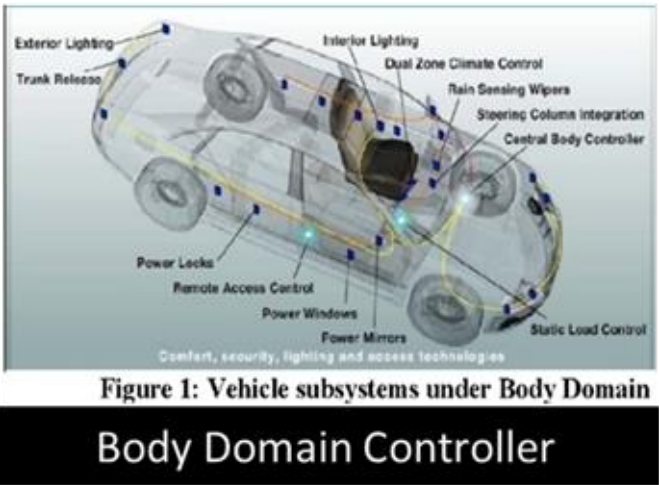
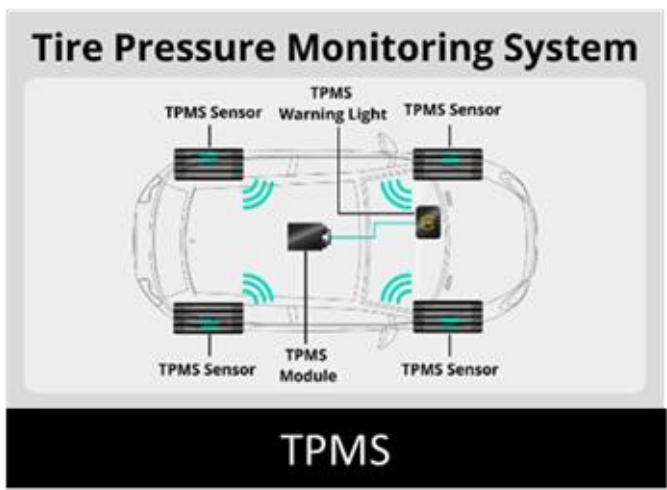
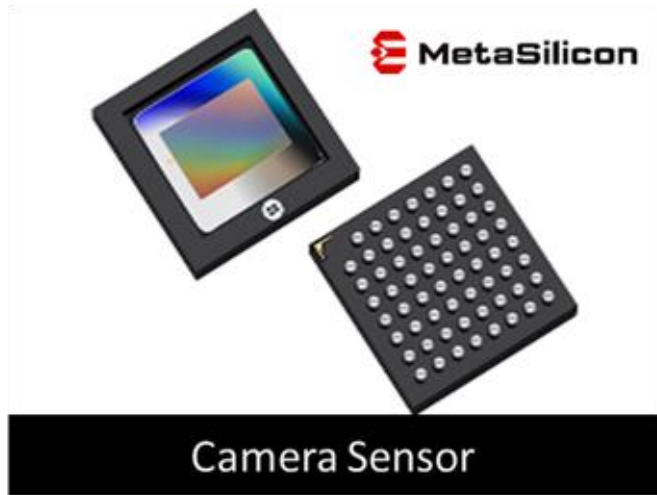
RISC-V will command 28% of the IoT market by 2025
Counterpoint, Sept 2021



The market size in the Artificial Intelligence market is projected to reach US\$305.90bn in 2024. The market size is expected to show an annual growth rate (**CAGR 2024-2030**) of **15.83%**, resulting in a market volume of US\$738.80bn by 2030.

RISC-V-based AI SoCs will grow 73.6% CAGR to 25B units and \$291B in revenue by 2027
Semico Research, Dec 2021

Andes Successful Story in Automotive



MTIA: Meta Training / Inference Accelerator

Powered by Andes AX25-V100 + ACE

- ISCA 2023 paper, “MTIA: First Generation Silicon Targeting Meta’s Recommendation Systems”
- Proc-A/B: AX25-V100, an early version of the popular NX27V
- Andes Custom Extensions: for new interfaces, instructions and registers
- Performs quite well on low and medium complexity models



Figure 3: High-level architecture of the accelerator

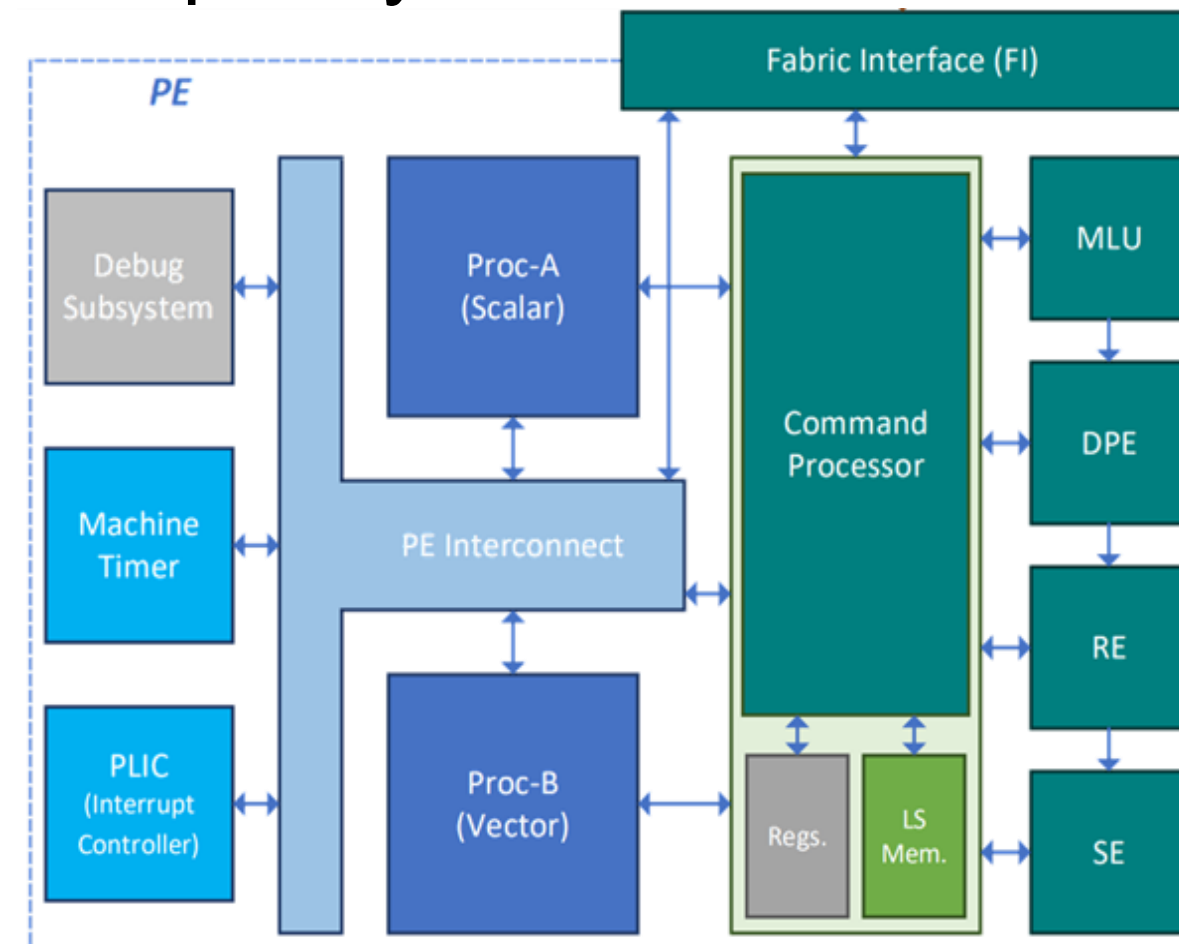
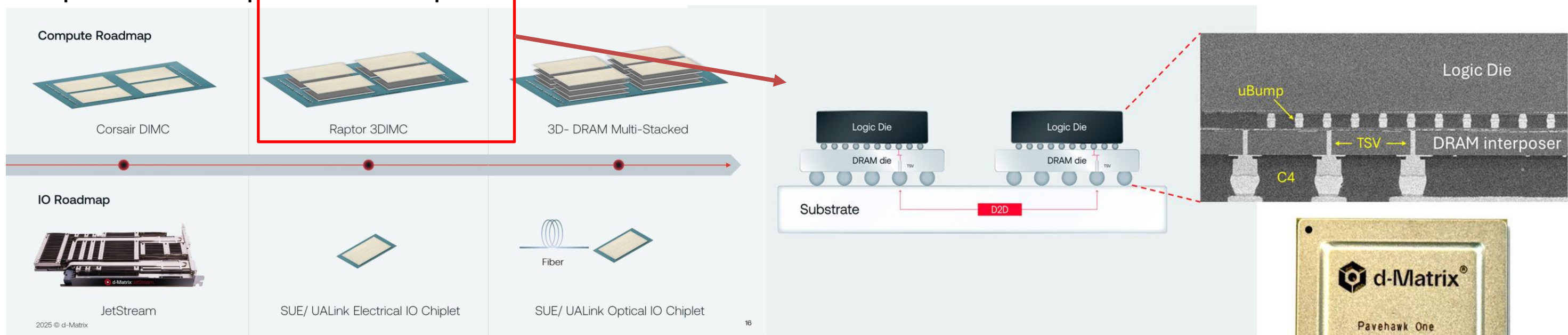


Figure 4: PE's internal organization

d-Matrix: Raptor Accelerator for Data-Center

Powered by Andes AX46MPV

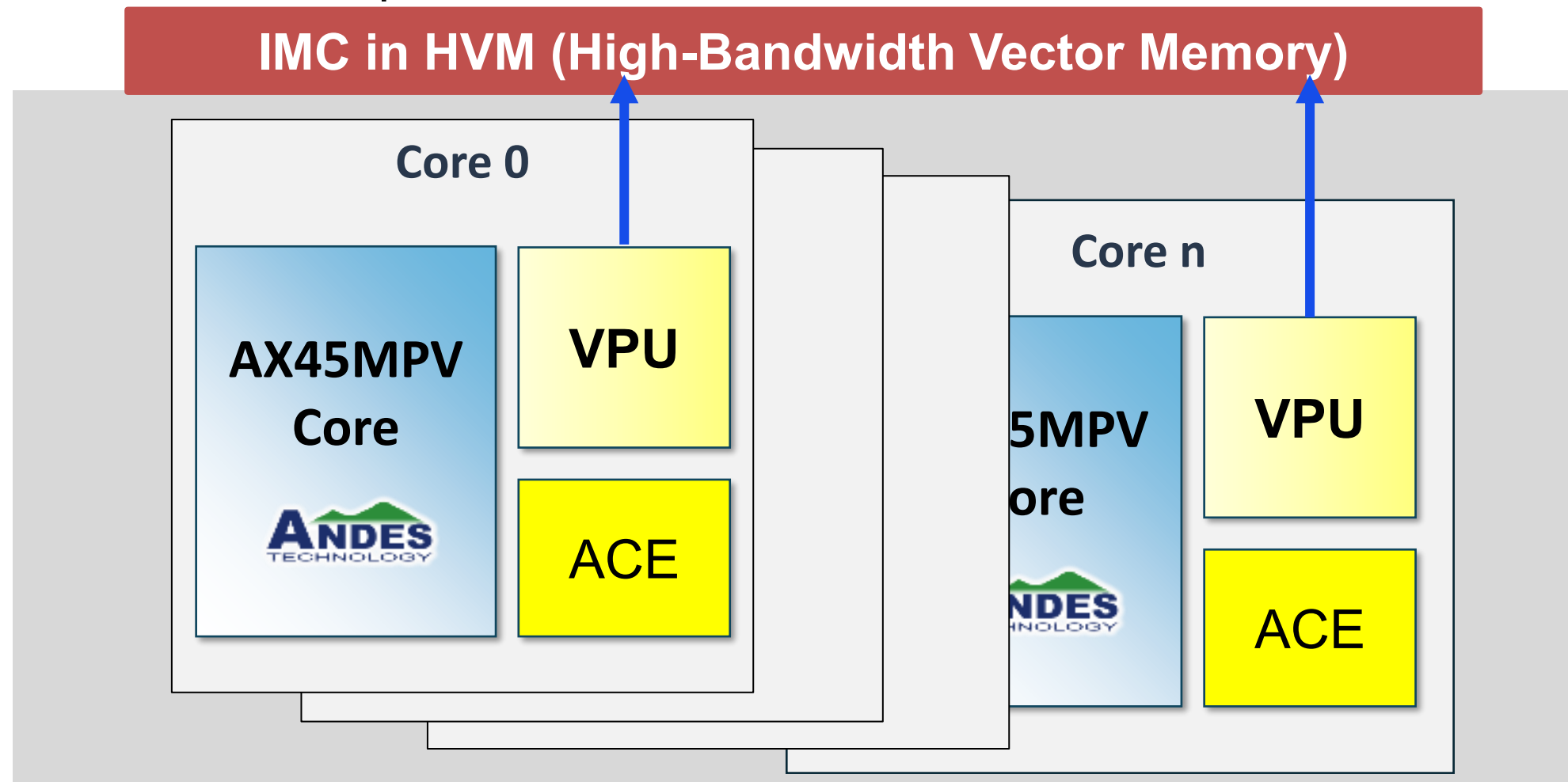
- The Raptor accelerator under development by d-Matrix will be the first to feature d-Matrix's revolutionary 3D In-Memory Compute (3DIMC™) technology. A highly efficient chiplet-based approach and the world's first 3D DRAM solution for AI inference at scale, 3DIMC stacks compute and memory to reduce the energy and latency of data movement by ten-fold, addressing the “memory wall” that limits conventional AI inference systems.
- By integrating the Andes' AX46MPV as both the orchestration and vector compute engine, Raptor gains the performance headroom and efficiency needed to push past traditional memory and power bottlenecks. Early results already show up to 2.3x performance improvement on key transformer kernels compared to our previous-generation core.
- “Raptor's innovative design is pushing inference efficiency and scalability far beyond what conventional architectures can achieve,” said Sid Sheth, Founder and CEO of d-Matrix. “The AX46MPV's RISC-V architecture provides the ideal CPU for our 3DIMC approach, allowing us to deliver datacenter-scale inference with unprecedented performance per watt.”



Fractile.ai: Compute-In-Memory

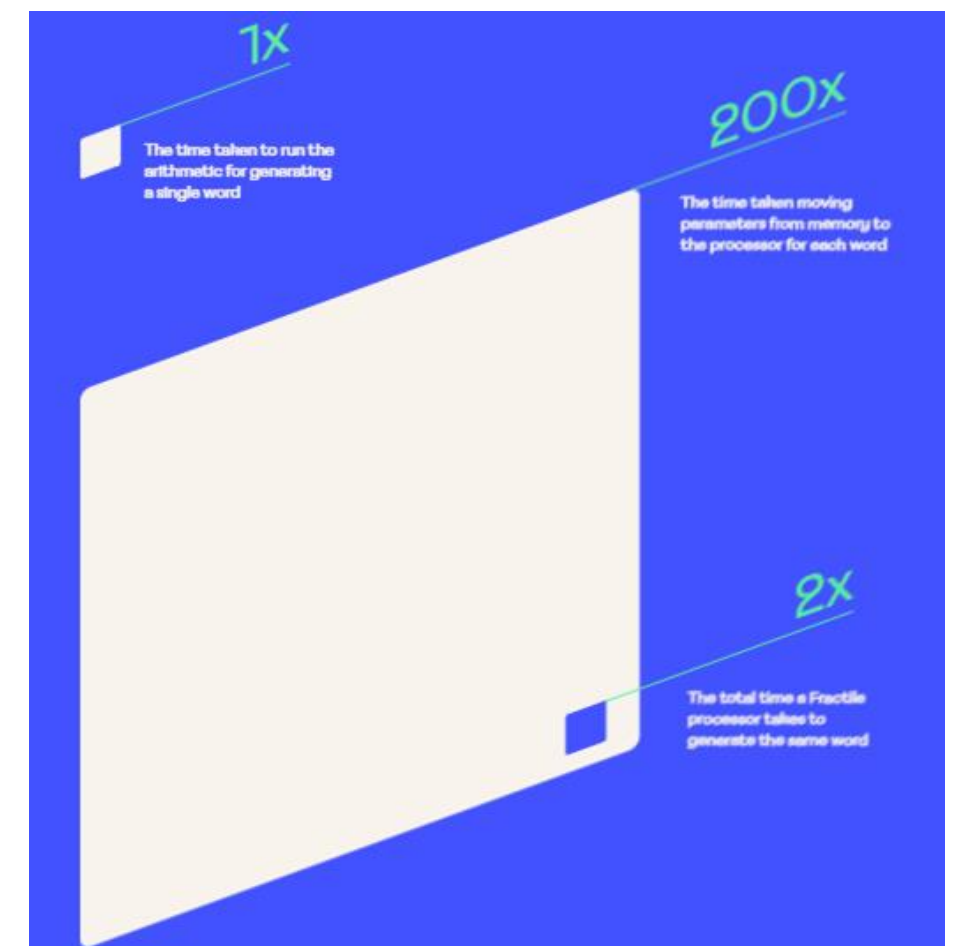
Powered by Andes AX45MPV + ACE

- Performing 100% of the operations needed to run model inference in memory
- Blast through the memory bottleneck
- Creative micro-architecture, support high performance multi-vector processors
- By using Andes AX45MPV and ACE, it can achieve the goal of accelerating mathematical computations



FRACTILE

100% In-Memory Inference
→ 200x Faster Memory Access



Edge AI with Computing In-Memory

- **Axelera** Metis SoC Targeting Computer Vision applications
- 4 powerful PE's, each with digital In-Memory Computing (D-IMC)
- RISC-V processors for both PE control as well as system control under Linux

Powerful



214 TOPS/chip, best in class performance, **2x-5x** throughput vs. new entrants*

Scalable & Future Proof

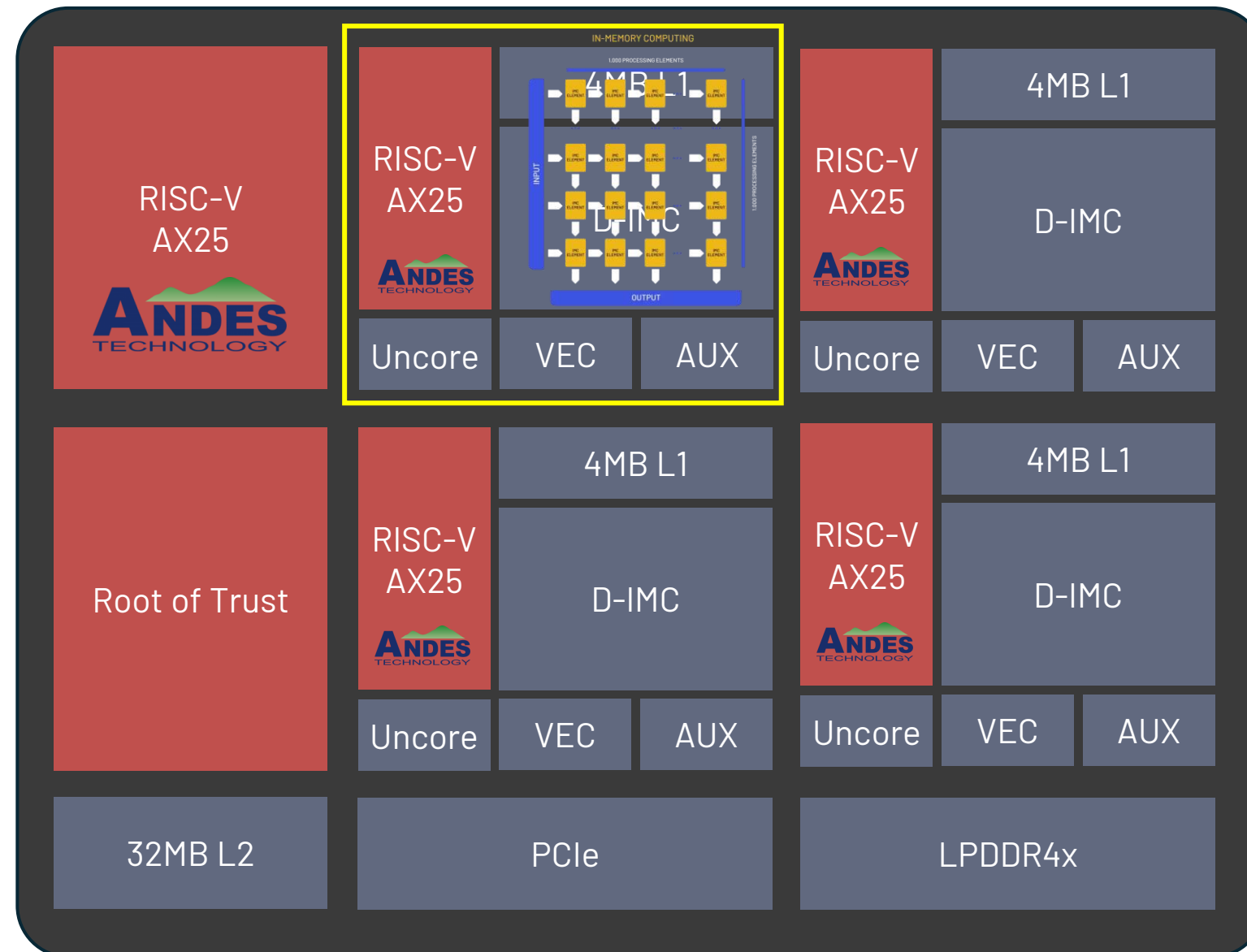


Programmable architecture and scalable multicore technology to support **future workload** such as **NLP & Generative AI**

Compatible



Working **with any CPU** or **operating system** for **fast hardware integration**



Competitive



Best performance/price **up to 10x vs. GPU**

Efficient



15 TOPs/W, **up to 5x vs. GPU** and market leaders*

Plug & Play

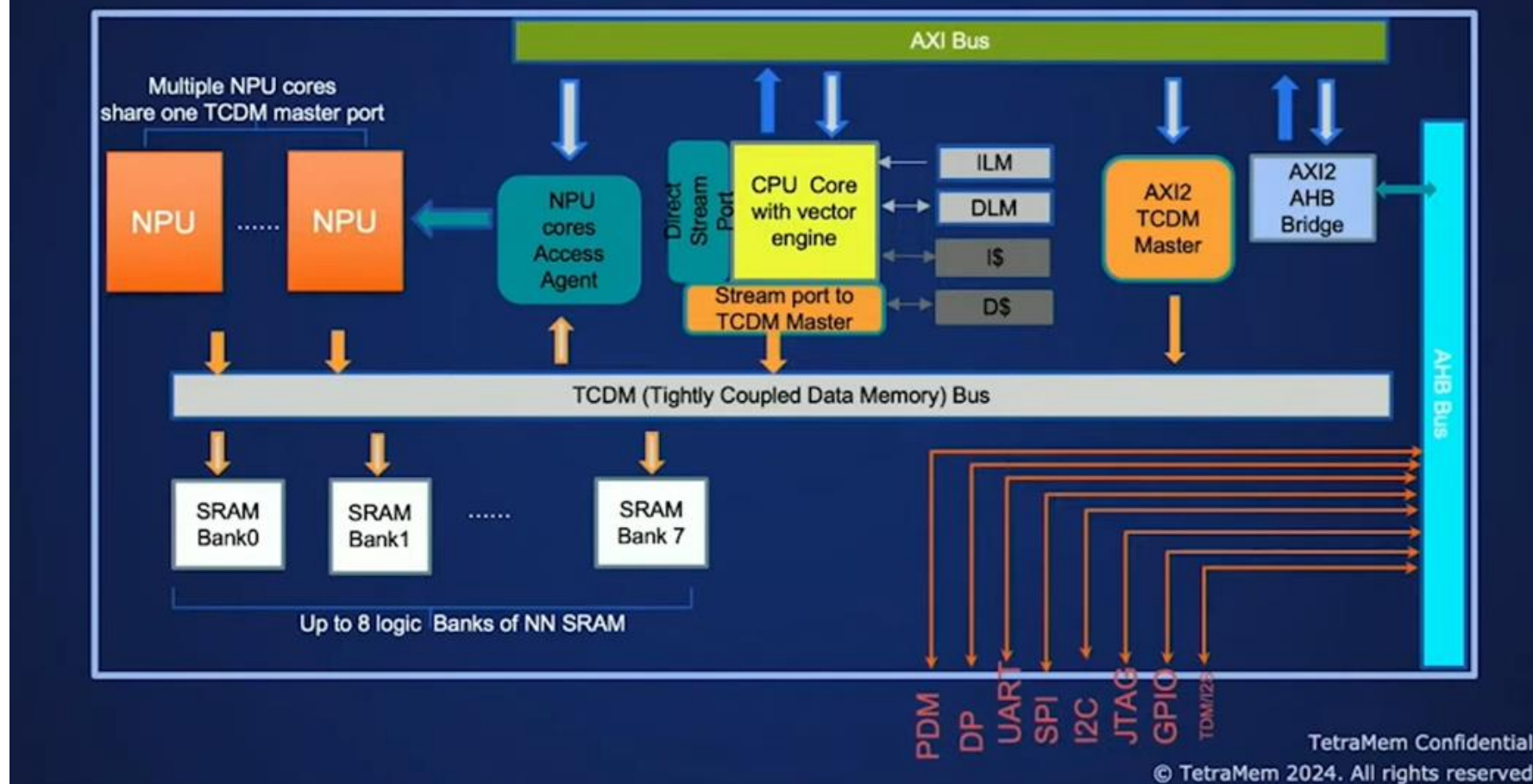


Compatible with AI frameworks, any OS, for **fast software integration**

Edge AI with Analog Computing In-Memory

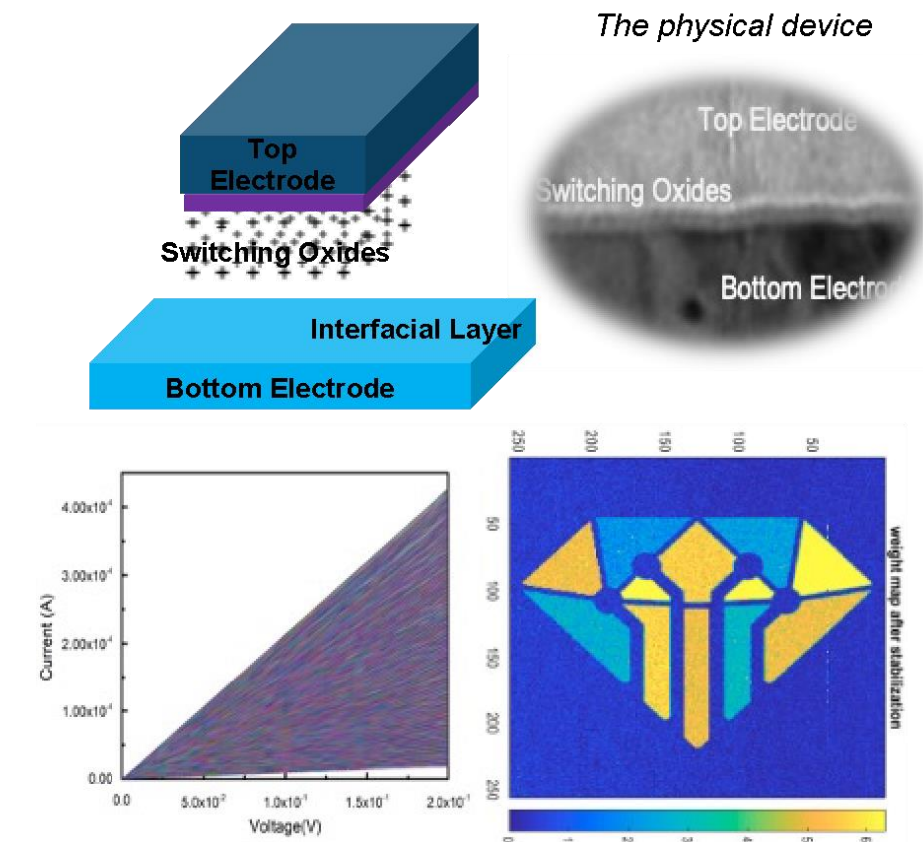
- **TetraMem** Analog Computing-In-Memory MX200 (**RRAM-based**)
- 8-bit 256x256 (64K) MAC Engines, **>30 TOPS/W** performance
- ML core operators (conv, gemm) processed in NPU
- Remaining operations processed in RISC-V Vector processors and control CPU

TetraMem NPU SoC MX200



8 bits multi-level
RRAM device

"Thousands of conductance levels in memristors monolithically integrated on CMOS" led by TetraMem, Nature, Mar 2023, <https://rdcu.be/c8GWO>



Endpoint AI Application

- **Renesas R9A06G150 Voice-Control ASSP**
 - With 100MHz DSP-capable D25F processor
 - ML-based voice recognition gets >50% speedup by using P-extension



Voice HMI ASSP

100MHz 32-Bit
RISC-V with DSP, FP ext.

VCC:2.7-3.6V
Ta: -40~85°C

 CPU

Andes-D25F
RV32ICMAPF

[Extensions]
Andes StackSafe,
PowerBrake,
Recoverable NMI,
Branch prediction

PMP 16 regions

 Memory

Code Flash (256 KB)
SRAM (128 KB)
[w/ 4x32KB power-off]

Data Flash (16 KB)
Standby SRAM (1 KB)

QSPI (1ch)

 Analog

12-bit ADC (6ch)
w/ 2 S/H

12-bit DAC (2ch)

 Timers

16-bit GPT (4ch)

32-bit Low Power Timer (4ch)

WDT

 Communication

SCI (2ch)
w/ FIFO, Manchester

I3C (1ch)

SPI (1ch) w/ FIFO

PDM (2ch)

SSIE (2ch)

IRDA (SCI0)

 System

Machine Timer

DTC

DMA (8ch)

On-chip Oscillators
(HOCO, MOCO, ILOCO)
Ext. Oscillator/Clock (MOSC)

32-bit DOC

 Safety

Bus Master MPU

SRAM Parity Check

Clock Accuracy Check

CRC Calculator

IWDT

Oscillation Stop Detection

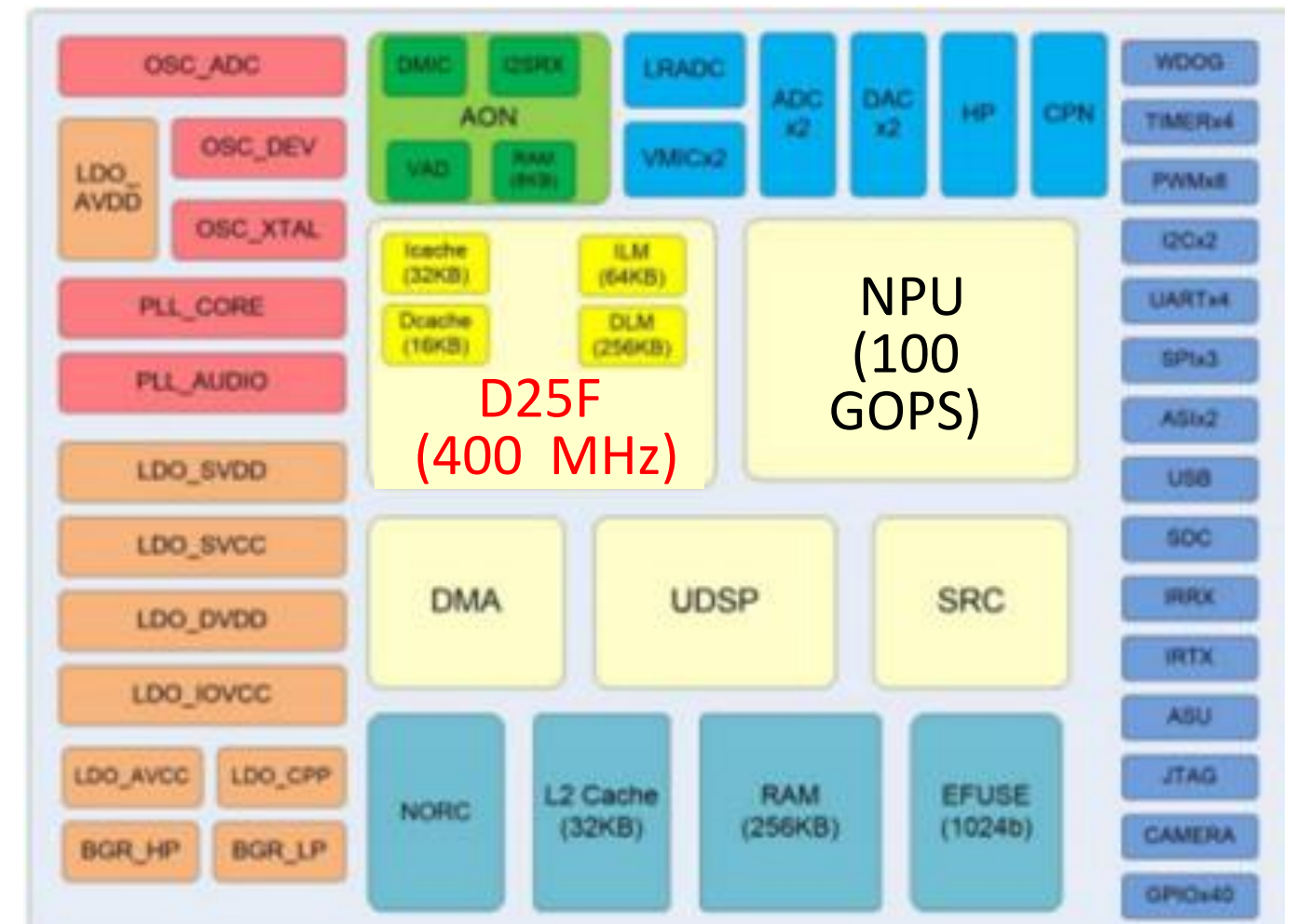
 Package

QFN 48
QFN 32
QFN 24

Endpoint AI

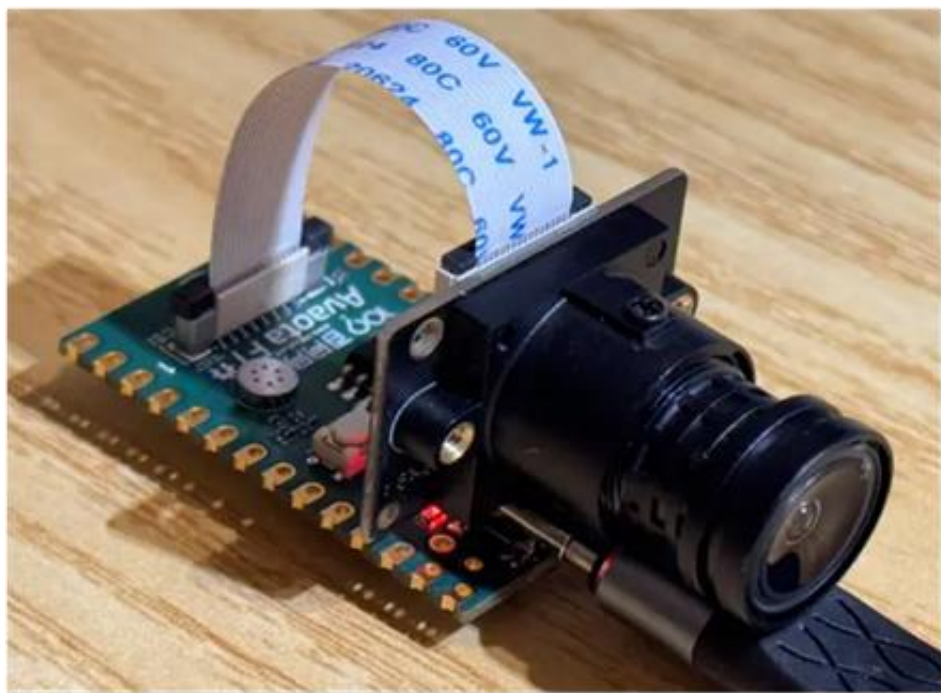
Spacetouch SPV60 Intelligent audio processor

- High performance for customer development
 - 100 GOPS NPU for noise reduction, echo cancellation, howling suppression
 - uDSP for FFT/IFFT, atan, log, etc.
 - 400MHz D25F with ID caches/Local Memory
- Rich audio interfaces and other peripherals
- Applications:
 - Intelligent voice, smart earphone, professional audio

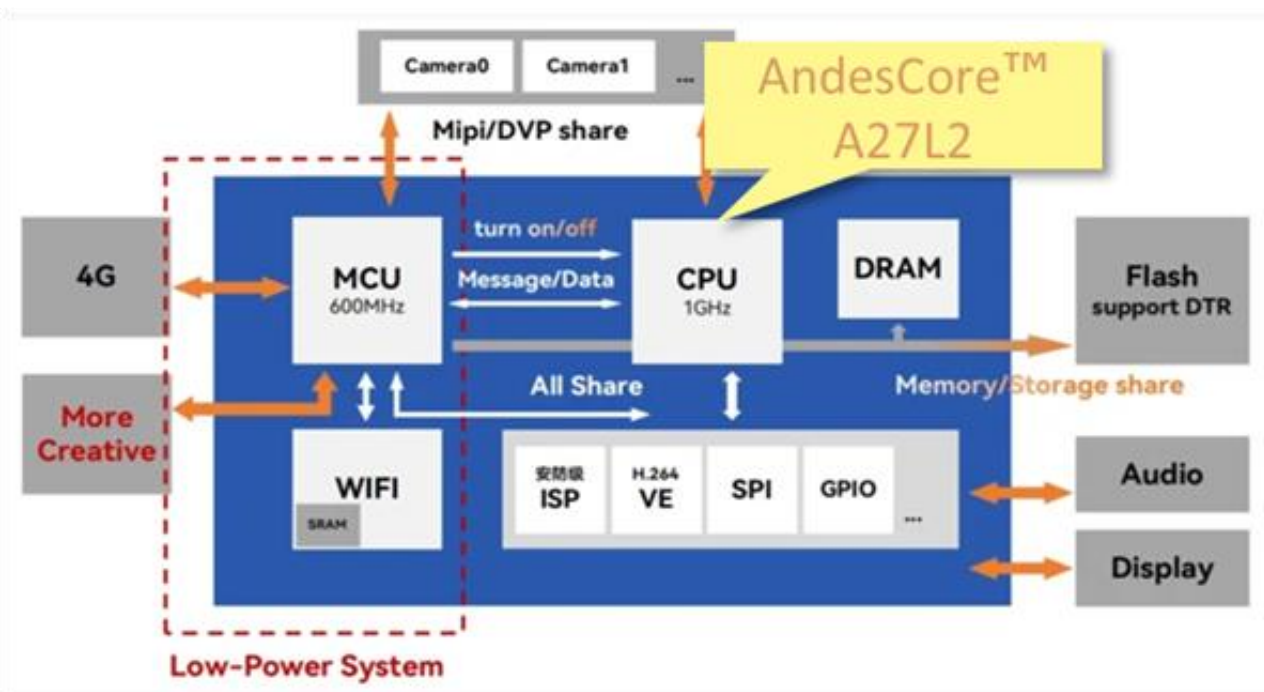


Allwinner Camera SoC

- The Avaota F1 is an ultra-small, open-source hardware Linux SBC powered by an Allwinner V821 32-bit RISC-V camera SoC with 64MB on-chip DDR2 and built-in 2.4 GHz WiFi 4, and designed for camera applications with a MIPI CSI connector.
- **1.2 GHz Andes A27L2 RISC-V CPU** is designed to handle features such as DRAM and storage, the 600 MHz RISC-V MCU manages WiFi and an optional 4G LTE module. Other features like H.264 VPU, cameras, GPIO, SPI, audio, etc.



Avaota F1 – A tiny camera board



Typical Allwinner V821 Application Diagram

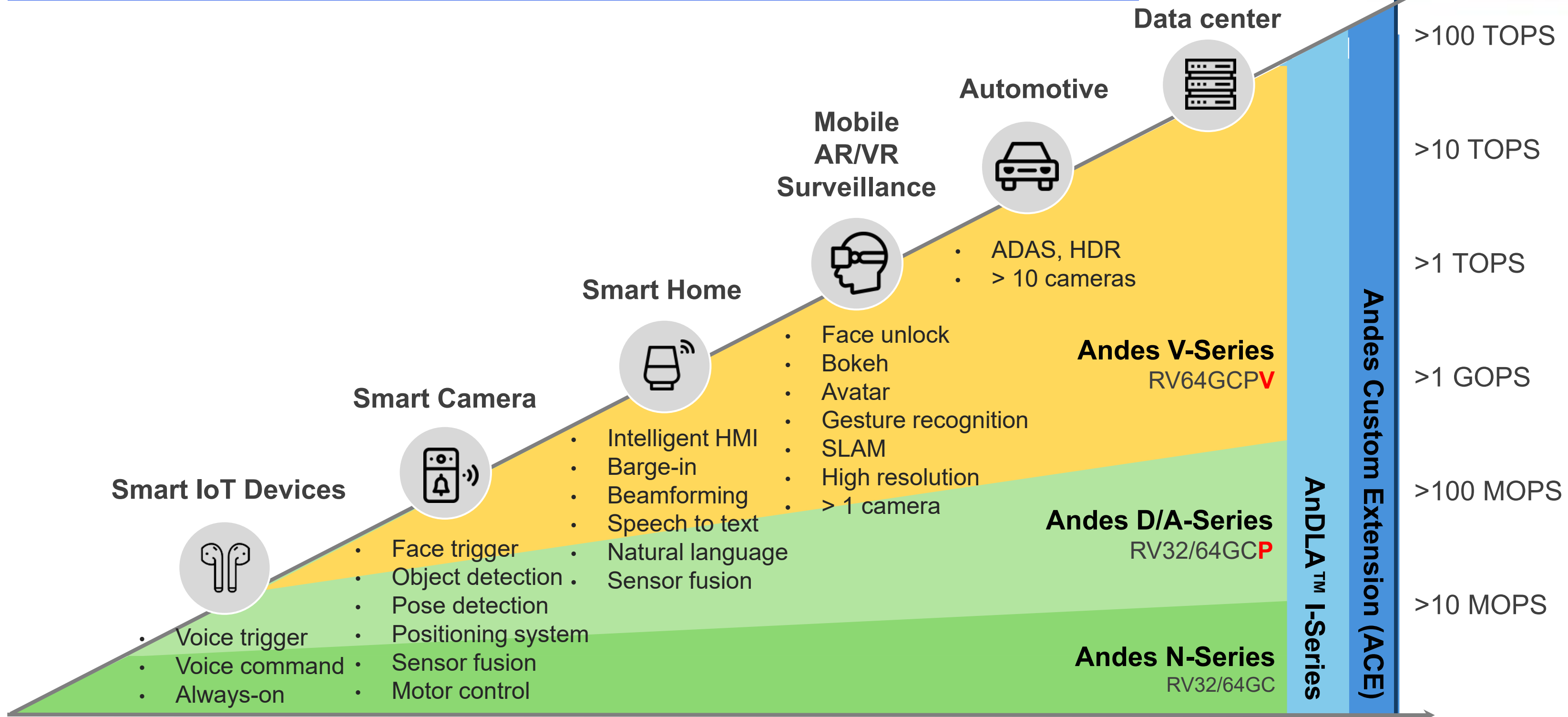


Allwinner V821 block diagram

The R&D Power for The Future



Andes RISC-V Processors to Fit Your AI



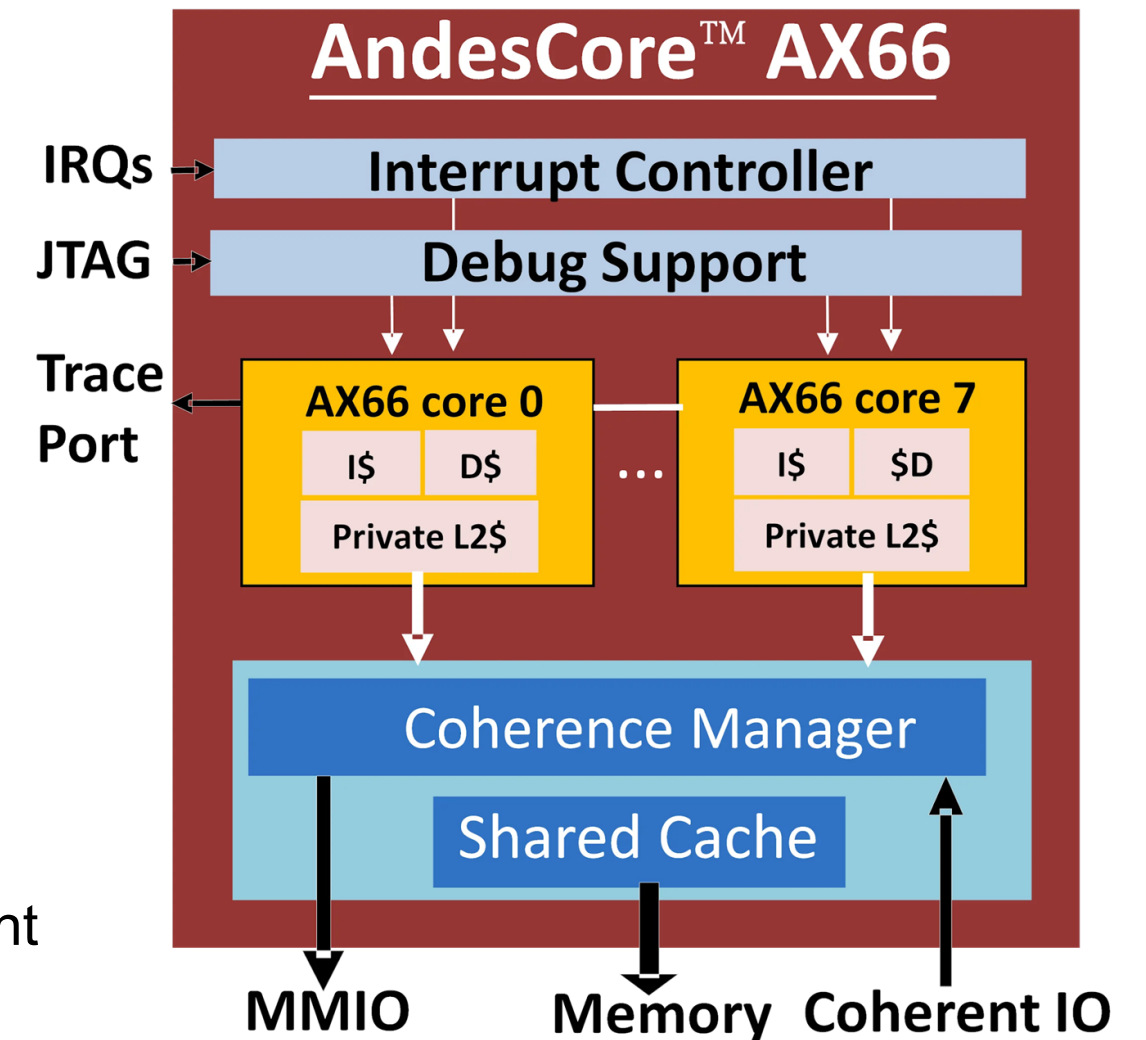
AndesCore™ RISC-V CPU

	General Purpose/Linux CPU					Vector/FuSa CPU	
	32-bit			64-bit			
	N- Baseline	D- DSP SIMD Accelerated Computing	A- MMU, Linux AP MP- SMP Multi-core 4/8/16 core	NX- Baseline	AX- MMU, Linux AP MP- SMP Multi-core 4/8/16 core	Vector Accelerated Computing VLEN up to 512/1024/2048	FuSa Functional Safety ASIL-B/ D
Cuzco Series Multiple execution pipeline					Cuzco RVA23+		Cuzco-SE
60 Series 13-stage Out of Order					AX65/AX66 Specint 2K6 (8.78 / 9.5)		
46 Series 8-stage Superscalar			A46MP (up to 16 cores)		AX46MP (up to 16 cores)	A46MPV (VLEN up to 256 bit) AX46MPV (VLEN up to 2048 bit)	AX46MPV-SE
45 Series 8-stage Superscalar	N45	D45	A45(MP)	NX45	AX45(MP)	AX45MPV (VLEN up to 1024 bit)	D45-SE (ASIL-B/D)
25/27 Series 5-stage Fast& Compact	N25F	D25F	A27(L2) A25(MP)	NX25F	AX27(L2) AX25MP	NX27V (VLEN up to 512 bit)	N/D25F-SE (ASIL-B)
22/23 Series 3-stage Fast& Compact	N225	D23					D23-SE (ASIL-B/D)

Andes' Advanced AndesCore™ AX66

AX66 Feature Overview

- 64-bit out-of-order 4 wide decode 13-stage CPU core with 128 reordering buffers and 8 functional pipelines
- Symmetric multiprocessing up to 8 cores
- Private L2 cache support
- Level-3 shared cache and coherence support
- AndeStar™ V5 Instruction Set Architecture (ISA)
- Compliant to RISC-V GCBV and Vector Cryptography
- Hypervisor(RVH)
- RVA23 profile compliant
- 64-bit architecture for memory space over 4GB
- TAGE Branch predication for highly accurate prediction
- Linux-capable Memory Management Unit (MMU)
- Physical Memory Protection (PMP) and latest architecture enhancement extension (ePMP) for access permission controls
- AIA with APLIC and IMSIC support
- ECC or Parity for SRAM error protection
- StackSafe™ hardware to help measuring stack size, and detecting runtime overflow/underflow
- PowerBrake and WFI (Wait for Interrupt) for different power saving occasions

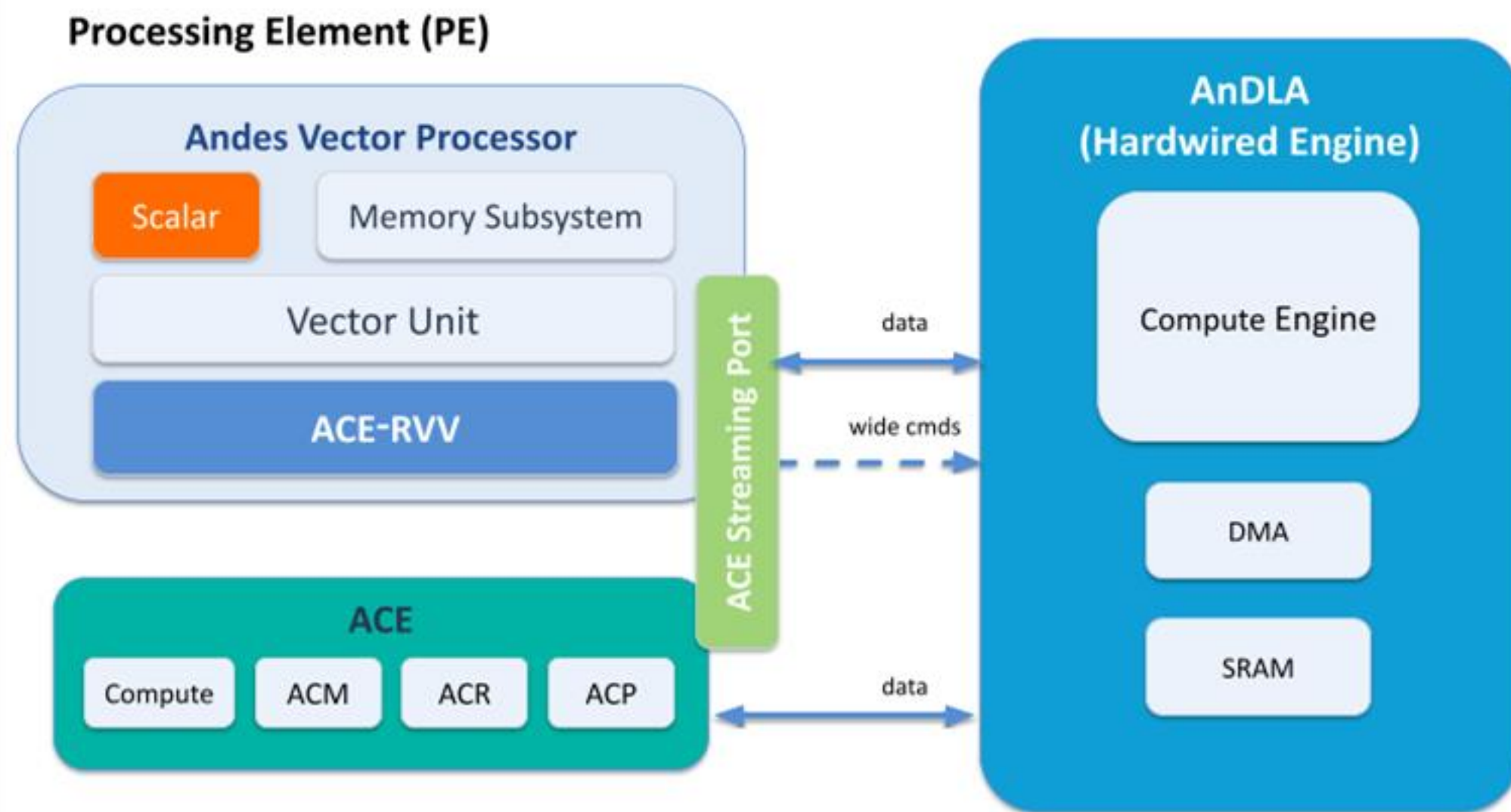


Key applications for the AX66 include:

1. Networking and Communications
2. Android Devices (including wearables, POS terminals, digital signage, and TV set-top boxes)
3. Video and Multimedia Processing
4. SmartNIC or DPU (Data Processing Units)
5. AI SoC (Systems on Chip)
6. Edge Servers
7. Edge/Data Center AI/ML Inference
8. Vision and Camera Applications

Expandable RISC-V AI Subsystem

- Extend with **Andes Custom Extension (ACE)**, ACE-RVV and ACE Streaming Port (ASP)
- **COPILOT** powerful tool for customers to define their own ISA
- **AnDLA**: Andes I-series Deep Learning Accelerator

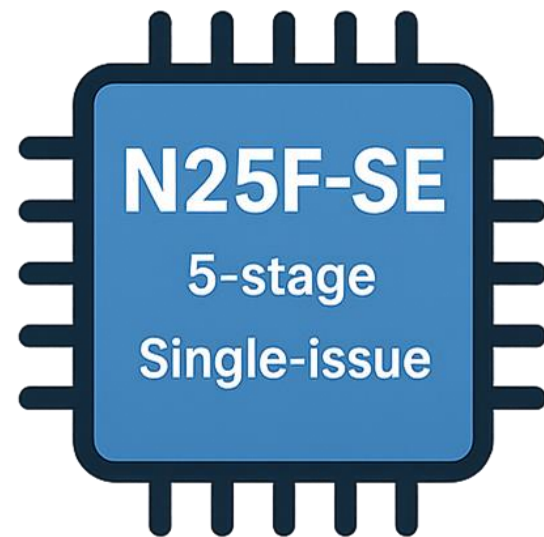


Expansion 1.
Compute

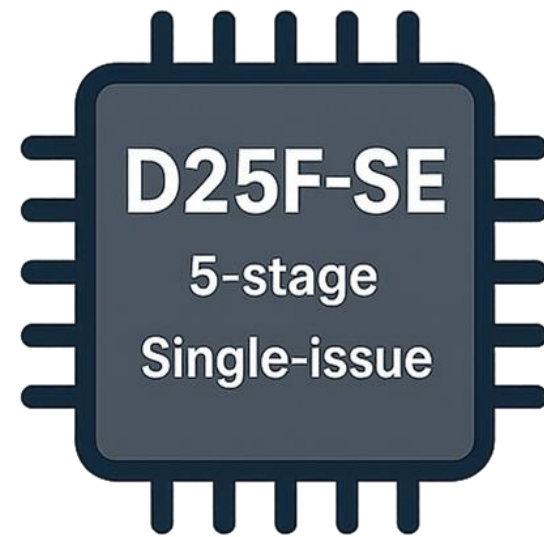
Expansion 2.
Data Transfer Efficiency

Expansion 3.
Control Signals

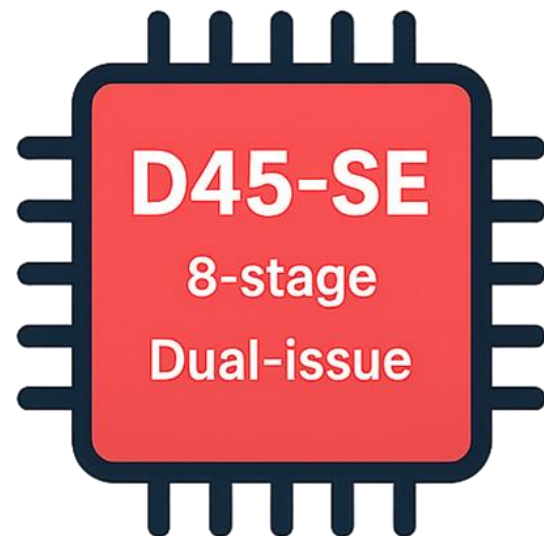
Safety Mechanisms Andes FuSA cores



Mainstream



Mainstream



Mission-Critical



Low Power & Security

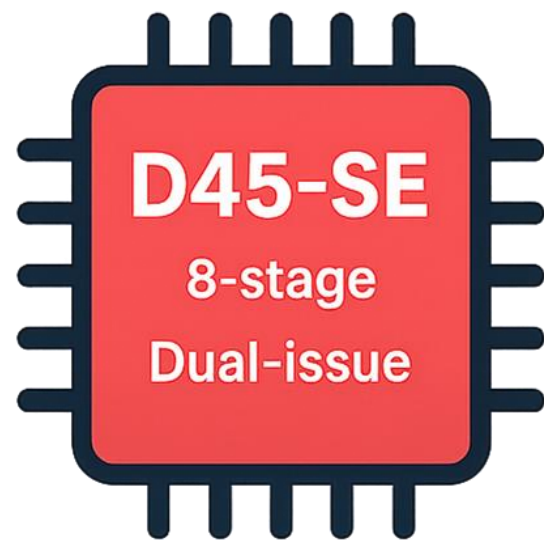
Common Safety Features

- Advanced ECC: address decoder, white-noise protection, error status
- Core trap status bus interface
- Stack protection: StackSafe
- NMI (non-maskable interrupt)
- PMP

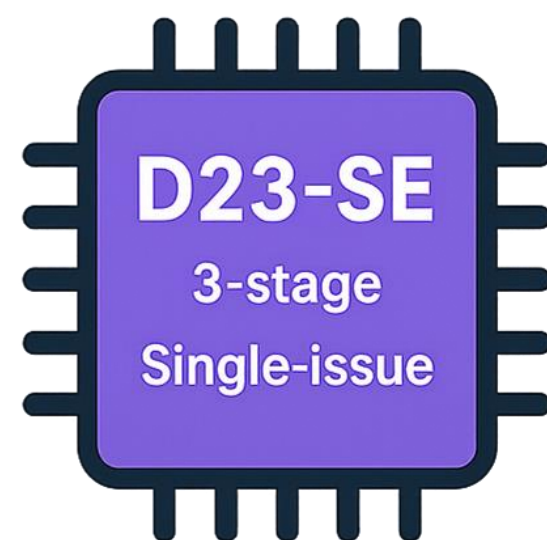
External Mechanisms

- WDT (watchdog timer)
- Software test library (STL)
- Partner: Resiltech — 

Safety Mechanisms Andes FuSA cores



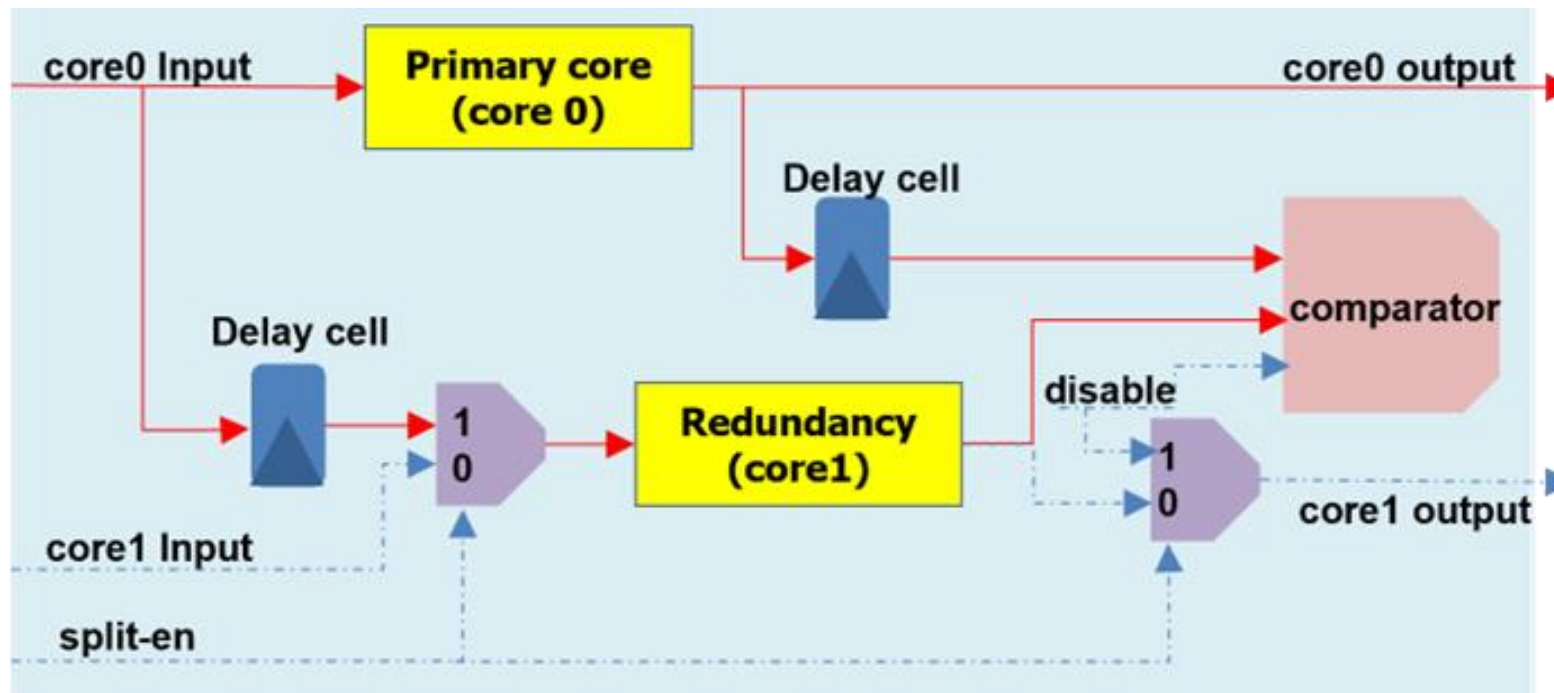
Mission-Critical



Low Power & Security

Applied on D45-SE & D23-SE

- Dual-core lockstep (DCLS)
- Bus protection:
 - Information redundancy
 - Frame counter
 - Timeout detection



AnDLA™ I-Series : I350 & I370

I350

- **CNN**
- i8i8 64/256/1024 MAC
(i8i8 = weight INT8, activation INT8)
- AXI-64
- 16KB-4MB SHRAM

Ethos-U55	• 256 MAC • Local SRAM 48KB • System SRAM MB-level	278,000	91.3
AnDLA I350	• 256 MAC • Local SRAM 256KB • No system SRAM	283,708	117.5

I370

v1.0

- **CNN, RNN (new OPs)**
- i8i8 64/256/1024 MAC
- **i8i16 MAC = i8i8 / 2**
- AXI-64/128/256
- **AHB-64**
- 16KB-4MB SHRAM

IP	Config	Logic Area um2 @12nm		
Neo110	• 64 MAC • Local SRAM 128KB	370,000	800.0	96.3
AnDLA I370	• 64 MAC • Local SRAM 128KB	227,083	4784.7	30.4

✓ Performance higher: **1.3x**

1. AnDLA I350 v1.0 official configuration: 2 EDP, SHRAM 16 banks, 40T DDR latency
2. The power is based on simulation measurements with Cadence Genusv 20.11, averaged analysis. To achieve lower power consumption, the HVT process is recommended.
3. The performance is estimated on FPGA
4. The area is with scan_factor:1.33, zwl_comb_scaling: 1.23, zwl_flop_scaling: 1.05, utilization 65%
5. Area Proc: 28nm, HVT, SS, 0.81V, 0C @ 500MHz

✓ Performance higher: **6.0x**

✓ Power lower: **3.2x**

✓ Area smaller: **1.6x**

- Note
- 1) AnDLA I370 configuration: 8 banks, 40T DDR latency
 - 2) Area estimation based on 12nm, SS 9T 0.9V SVT -40C @1.2GHz, zwl_scaling: 1.25, scan_factor: 1.25, utilization 60%
 - 4) The cycle counts are estimated results based on architectural considerations of mixed FPGA

AndeSight™ Software Components

			standard features
Optimizing Compilers • GCC and LLVM optimized for AndeCores	Meta Linker Script Editors	Advanced SoC Debug Support • Bit field display • Exception handing • Instruction tracer	Analysis • Function profiling • Code size analysis
Advanced Libraries • DSP and math functions optimized for RVV and RVP	AndeCore Simulators • AndeSim • QEMU advanced features (separately licensable)	RTOS/Linux Support • OS-aware debugging • Device Drivers	Sample Projects • Demonstrate features for RISC-V ISA and AndeCores
AutoOPTune • Automatic compiler flag tuner	AndeSysC • AndeCore SystemC library and sample SoC	AndesClarity • Processor pipeline analyzer/visualizer	Andes Custom Extensions™ (ACE) • Automated generation of toolchains, ISS and RTL for user extensions

RISC-V International Major Members



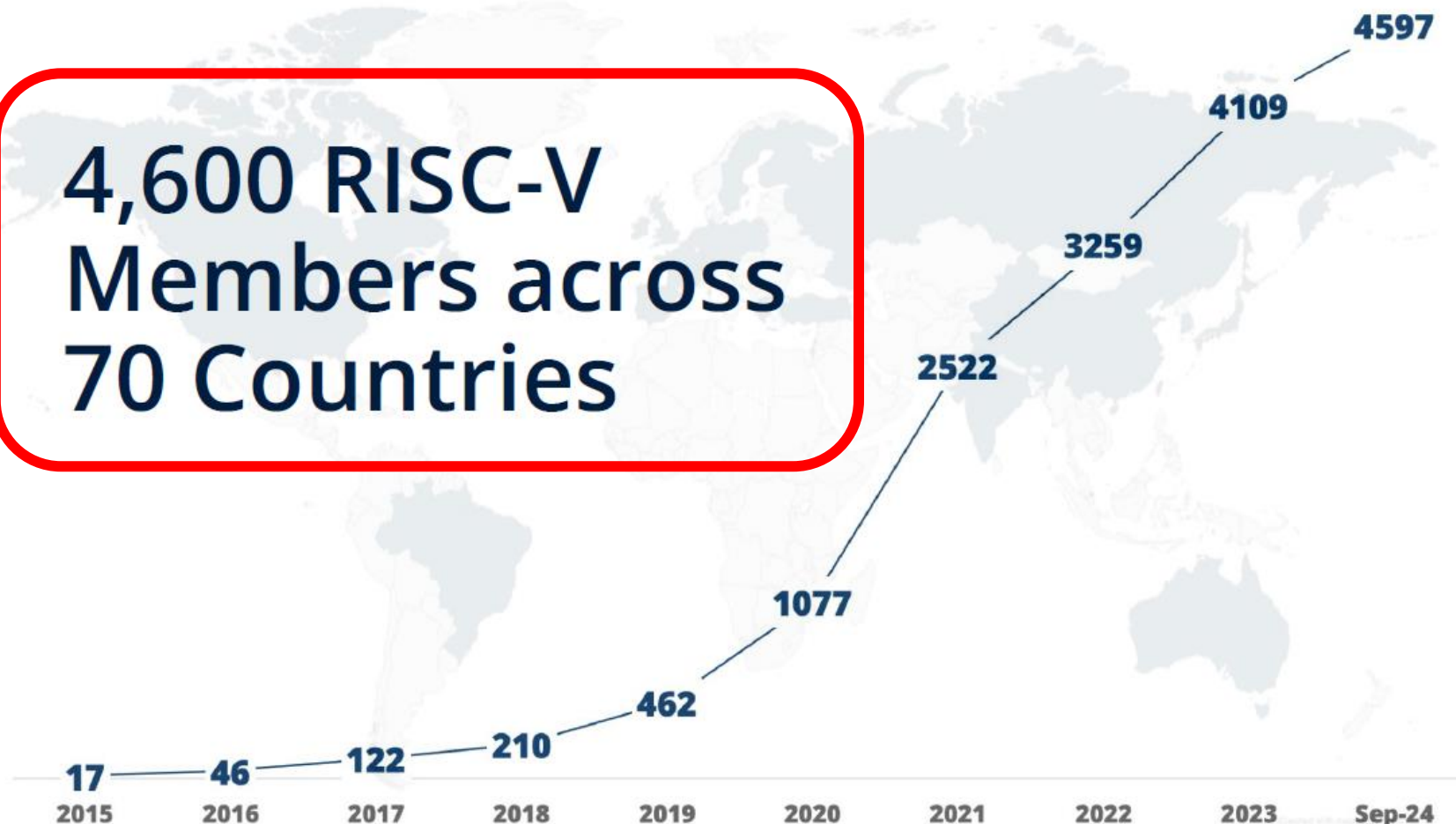
Andes Automotive Ecosystem

Safety RTOS & STL	AUTOSAR	Security / HSM	Compiler / Debugger / Tool
 WITTENSTEIN  Microsoft WNRDRVR  RESILTECH	 VECTOR  恒润科技 HIRAN TECHNOLOGIES  普华基础软件 SIEMENS  KopherBit  Fpt Software	 繁盛微电子 FORESEMI SECURE-IC THE SECURITY SCIENCE COMPANY Rambus Virtual Open Systems PUFsecurity TrustKernel  豆荚 Beanpod	 LAUTERBACH DEVELOPMENT TOOLS  ASHLING  Green Hills SOFTWARE  LDRA ASSURED TASKING PARASOFT

Andes Partners and RISC-V Ecosystem

Category	
IP	SECURE-IC THE SECURITY SCIENCE COMPANY L&T Technology Services Rambus Veridify Security Mentor Graphics CYPRESS PERFORM DMP DIGITAL MEDIA PROFESSIONALS EXPERT VIDEO ACQUISITION Rafael Micro CRYPTO QUANTIQUE DOLPHIN INTEGRATION Dolphin Technology Tiempo SECURE ememory ATTOPSEMI™ Technology TECHNOLOGIA IntelliProp dxcorr Imagination 繁盛微电子 FORESEM menta M31 DOVER MICROSYSTEMS csem PUF security Kneron SKYECHIP expedera SIGNATURE IP CORPORATION FLoadin ORCA SYSTEMS CEVA mobiveil Investors in Innovation™ Aett Think Silicon ultra-low power vivid graphics
SW and Dev Env.	KopherBir LAUTERBACH DEVELOPMENT TOOLS Micrium® Embedded Software SEC Leading Innovation in the Fineflt eForce CooCox expresslogic LDRA ARPHIC Aplix Corporation CO-OPERATION Virtual Open Systems TrustKernel 上海通钰信息科技有限公司 interniche technologies, inc. RealTimeLogic CIDAA Mentor Graphics SylixOS® embedded multicoreware MICROTIME PARASOFT altix WITTENSTEIN CS solutions R&W Green Hills® SOFTWARE Micro Digital RELJET RTOS VectorFabrics Cyberon Leading Speech Solution Provider 柏霖科技股份有限公司 Portallinks Technology Co., Ltd. OPEN CONNECTIVITY FOUNDATION wolfSSL TUXERA tech J&D Tech Co. Ltd. OPEN AI LAB 开放智能 SEGGER Orbweb clarinox Verifysoft TECHNOLOGY TASKING PEAKHILLS ZAYA sensory iar ATs 卓尔科技 TeraPines 兆松科技 codeplay ASHLING Grovety Inc. People and hardware connecting technologies
Design Service, Foundries, EDA and others	alchip CMSC FARADAY GUC SMIC UMC BAYSAND eShard SOCLE FICUS DATA 讯息数据 HEJIAN tsmc incentia SiEn NSW NIPPON SYSTEMWARE CO., LTD. PGC ChipMotion 芯聚 MEIC Device WebAPI Consortium APLabs CSMC 摩尔精英 MooreElite.com CIRCUIT SUTRA TECHNOLOGIES PerfectVIPs Right Tools... Perfect Chip keyASIC Kaviaz 微核科技股份有限公司 cadence 茂積股份有限公司 MAOJET TECHNOLOGY CORP. SymMiD MindMotion SoC Solutions GLOBAL FOUNDRIES EMBC Truechip 聯興微系統科技 UniSense XtremeEDA Mentor Graphics

**4,600 RISC-V
Members across
70 Countries**



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SoC, IP, FPGA

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ODM, OEM

3 I/O
Memory, network, storage

18 Industry
Cloud, mobile, HPC, ML, automotive

22 Services
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Universities, Labs, other alliances

54 Software
Dev tools, firmware, OS

4.2k Individuals
RISC-V engineers and advocates

Sep 2024 update



Thank you